

# analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

MIXED-SIGNAL PROCESSOR MERGES DSP WITH ADC & DAC (page 3)

CMOS multiple Line Drivers & Receivers for RS-232 & RS-422 (page 8)

Choice of 12-Bit ADCs to convert in 500, 750, 1,000 ns (page 16)

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# Editor's Notes

## $\Sigma$ - $\Delta$ OR $\Delta$ - $\Sigma$ ?

This is not the most earth-shaking of controversies, and many readers may wonder what the fuss is all about—if they wonder at all. The issue is important to both editor and readers because of the need for consistency; we'd like to use the same name for the same thing whenever it appears. But *which* name? In the case of the modulation technique that led to a new oversampling *a/d* conversion mechanism, we chose *sigma-delta*. Here's why.



Ordinarily, when a new concept is named by its creators, the name sticks; it should not be changed unless it is erroneous or flies in the face of precedent. The seminal paper on this subject was published in 1962,<sup>1,2</sup> and its authors chose the name "delta-sigma modulation," since it was based on *delta* modulation but included an integration (summation, hence  $\Sigma$ ).

*Delta-sigma* was apparently unchallenged until the 1970s, when engineers at AT&T were publishing papers using the term *sigma-delta*. Why? According to Hauser,<sup>2</sup> the precedent had been to name variants of delta modulation with adjectives preceding the word "delta." Since the form of modulation in question is a variant of delta modulation, the sigma, used as an adjective—so the argument went—should precede the delta.

Many engineers who came upon the scene subsequently used whatever term caught their fancy, often without knowing why. It was even possible to find *both* terms used interchangeably in the same paper. As matters stand today, sigma delta is in widespread use, probably for the majority of citations. Would its adoption be an injustice to the inventors of the technique?

We think not. Like others, we believe that the name delta sigma is a departure from precedent. Not just in the sense of grammar, but also in relation to the hierarchy of operations. Consider a block diagram for embodying an analog root-mean-square (finding the square root of the mean of a squared signal) computer. First the signal is squared, then it is integrated, and finally it is rooted.



If we were to name the overall function after the causal order of operations, it would have to be called a "square mean root" function. But naming it in order of the *hierarchy* of its mathematical operations gives us the familiar—and undisputed—name, *root mean-square*. Consider now a block diagram for taking a difference (delta), then integrating it (sigma).



<sup>1</sup>"A Telemetry System by Code Modulation— $\Delta$ - $\Sigma$  Modulation," by H. Inose, Y. Yasuda, and J. Murakami, *IRE Transactions on Space Electronics Telemetry*, vol. SET-8, pp. 204-209, Sept. 1962.

<sup>2</sup>We are indebted to Prof. Max Hauser, of Cornell University's School of Electrical Engineering, for communicating to us the results of his research into this question. Much of the historical information in this column is based on his (as yet) unpublished notes.

Its causal order would give *delta sigma*, but in functional hierarchy it is *sigma delta*, since it computes the integral of a difference. We believe that the latter term is correct and follows precedent; and we have adopted it as our standard.

Dan Sheingold

## THE AUTHORS

**Amy Mar** (page 3) is Manager of Technical Publications for Analog Devices' DSP Division. She holds BSEE and MSEE degrees from Stanford University. Prior to joining ADI in 1986 she had been a product engineer at Intel Corporation and a contract technical writer. She enjoys the outdoors, cartoons, and cats.



**Lew Counts** (page 11) is a Fellow and Director of the Amplifier Group at Analog Devices Semiconductor. For the past 20 years at Analog Devices, Lew has designed—and managed the design of—a wide variety of amplifiers and analog signal-processing circuits, and has written numerous papers and articles. He is a graduate of MIT. Lew's favorite recreations are cross-country skiing and photography.



**Mark Murphy** (page 11) is a Senior Design Technician for the Amplifier Group at ADS. His responsibilities include providing lab support for the Amplifier Design Group and preparing new-product data sheets. Mark graduated with an ASEE from Moylish College, Limerick, Ireland; and he is completing his BSEE at Northeastern University. His interests include rowing, soccer, and beer brewing.



**Denis Regimbal** (page 3) is now Strategic Marketing Manager for fixed-point products at ADI's DSP Division. His photo, and a biographical sketch, appeared in volume 23, number 2.

**Bill Schweber** (page 8) is a Senior Technical Marketing Engineer at ADI, and Contributing Editor to *Analog Dialogue*. His photo, and a biographical sketch, can be found in volume 23, number 3.

**James Bryant** (page 20) is European Applications Manager for Analog Devices, based in Newbury, England. His photo and a biographical sketch appear in *Analog Dialogue* 23-2.

(more authors on page 22)

# analog dialogue

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106  
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# MIXED-SIGNAL PROCESSOR MERGES DSP WITH A/D, D/A CONVERTERS

## ADSP-21msp50 combines ADSP-2101 core and analog I/O

### Architecture is well-suited for embedded signal-processing applications

by Amy Mar and Denis Regimbal

The ADSP-21msp50\* is a general-purpose mixed-signal (analog plus digital) processor designed for interfacing to real-world signals with bandwidths from dc to 4 kHz. Well-suited for voiceband applications, such as digital mobile radio, telecommunications, voice synthesis, and voice compression, it is also appropriate in such applications as sonar, medical instrumentation, and adaptive filtering to cancel acoustic and low-frequency repetitive noise.

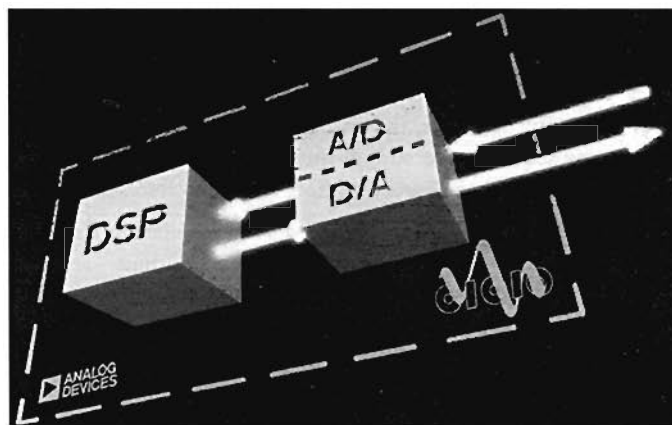
The evolution of digital signal processors is reminiscent of the way in which early microprocessors evolved into numerous specialized versions, each optimized for unique application requirements. For example, the 8051 microcontroller, a descendant of the 8080 microprocessor, incorporates integrated I/O for use as an embedded controller in appliances, VCRs, and smart devices.

Prior to the introduction of the ADSP-21msp50, embedded digital signal processing for analog signals required analog-to-digital and digital-to-analog data converters, along with the processor IC. For many applications, the combination is relatively costly and often consumes excessive amounts of board space and power. This made unfeasible many real-world signal processing applications for which DSP techniques were otherwise highly desirable.

The ADSP-21msp50 mixed-signal processor (MSProcessor™), based on Analog Devices' ADSP-2100\* family<sup>1,2,3,4</sup> of digital signal processors, incorporates both a/d and d/a conversion on a single CMOS chip. This level of integration provides new opportunities for building mixed-signal processing into dedicated applications, i.e., where the application-specific program code is fixed and transparent to the final end user. But the DSP algorithms themselves are often *adaptive*, adjusting key parameters to the specific conditions of the application.

## ARCHITECTURE OVERVIEW

An outgrowth of Analog Devices' ADSP-2100 family of fixed-point DSP processors, the ADSP-21msp50 has the same basic architecture, including two data address generators, a program sequencer and three paralleled computation units: an arithmetic and logic unit (ALU), a multiplier/accumulator (MAC), and a barrel shifter. In addition, like the ADSP-2101, the ADSP-21msp50 also contains static RAM: 2K words × 24 bits of program memory plus 1K words × 16 bits of data memory; and it has two synchronous serial ports and a 16-bit timer. It adds an a/d converter with 65-dB signal-to-noise ratio (SNR) and total harmonic distortion (THD), a d/a converter, and an 8- or 16-bit host interface port.



The common basic architecture of the ADSP-2100 family of processors is designed for coding and execution of algorithms with increased efficiency, aimed towards maximizing signal-processing performance. Figure 1 is a block diagram of the ADSP-21msp50 mixed-signal processor.

The diagram shows the three computation units: a 16-bit MAC with a 40-bit accumulator, a 16-bit ALU, and a barrel shifter. Each can feed back its own output, as well as feeding the processor's main data bus and an R (results) bus that has direct input to the other units. This allows essentially independent parallel operation of all units within an instruction cycle. The ADSP-21msp50's two independent address generators can fetch two operands per instruction cycle, while maintaining circular buffers and indexing without software overhead. The on-chip program sequencer supports zero-overhead interrupts, plus looping and branching to take advantage of the repetitive nature of DSP algorithms.

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<sup>1</sup>Fine, Bob, and Mike Nell, "Fast, Flexible CMOS Single-Chip  $\mu$ P for Digital Signal Processing." *Analog Dialogue* 20-2, 1986, 3-6.

<sup>2</sup>McQuaid, Jim, and Denis Regimbal, "Advanced Microcomputer is Optimized for DSP." *Analog Dialogue* 23-2, 1989, 3-6.

<sup>3</sup>Higgins, Richard J., *Digital Signal Processing in VLSI*. Englewood Cliffs, NJ: Prentice Hall, 1990.

<sup>4</sup>Mar, Amy, ed. *Digital Signal Processing Applications Using the ADSP-2100 Family*. Englewood Cliffs, NJ: Prentice Hall, 1990.

\*Use the reply card for technical data.

The ADSP-2100 family of processors is optimized for digital signal-processing (DSP) and other high-speed numeric processing applications. Digital signal-processing demands high performance, of which speed of executing instructions is but one component (*Analog Dialogue* 24-1). In evaluations, DSP architectures are distinguished from those of other types of microprocessors and microcontrollers by how well they perform in the following areas:

- **Fast and flexible arithmetic:** the ADSP-2100 family provides single-cycle multiplication (with and without accumulation), arbitrary amounts of shifting, and standard arithmetic and logical operations. Furthermore, the arithmetic units allow for computation in any sequence; because of this, a given DSP algorithm can be executed straightforwardly without awkward reformulation.
- **Extended dynamic range on multiplication/accumulation:** Extended sums-of-products—very common in DSP algorithms—are supported by the ADSP-2100 family. A 40-bit accumulator provides protection against overflow in successive accumulations to ensure that no loss of data or range occurs. Special instructions facilitate block-floating-point scaling of data.
- **Single-cycle fetch of two operands (from either on- or off-chip):** In extended sums-of-products calculations, two operands are needed to feed the calculation. ADSP-2100 family members are able to provide two-operand data throughput in a single cycle.
- **Hardware circular buffers (for both on- and off-chip data):** A large class of DSP algorithms, including most filters, requires circular buffers in order to realize maximum efficiency. ADSP-2100-based processors provide hardware to handle address pointer wrap-around, reducing overhead (thereby increasing performance) and simplifying implementation.
- **Zero-overhead looping and branching:** DSP algorithms are repetitive and are compactly expressed as loops. ADSP-2100-based processors support looped code with zero overhead, combining excellent performance with clear and easy-to-formulate programs. Furthermore, there are no overhead penalties for conditional program flow on ADSP-2100 based processors.

## KEY FEATURES

The ADSP-21msp50 differs from earlier ADSP-2100 family members by its dynamically reconfigurable host interface port, the a/d and d/a converters, and its additional power-down features.

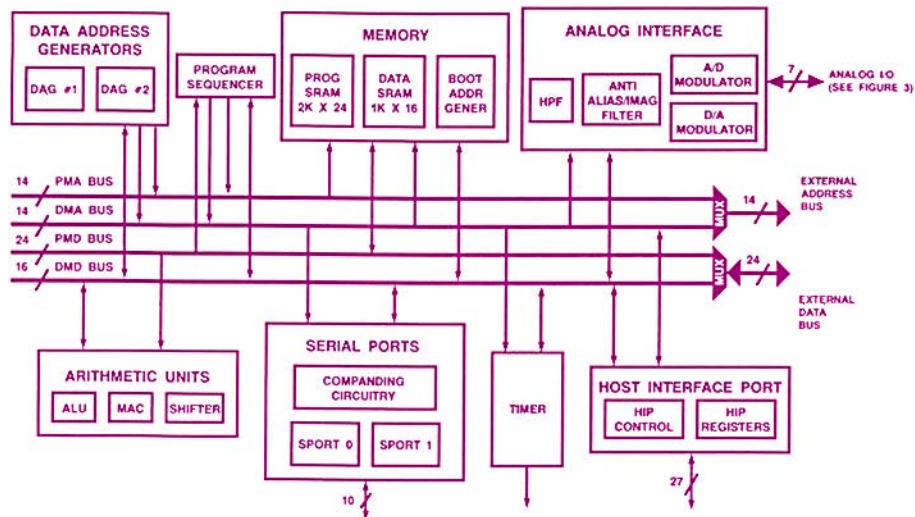


Figure 1. ADSP-21msp50's internal block diagram.

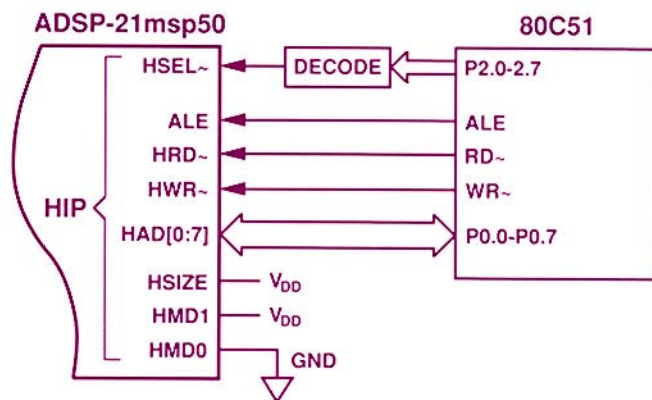


Figure 2. Host interface port configured for the 80C51 microprocessor family.

**Host Interface Port:** The ADSP-21msp50 host interface port (HIP) is a parallel I/O port for interfacing the ADSP-21msp50 to a host processor, such as the Intel 8051 and Motorola 68000 families (Figure 2). Through the flexible host interface port, the ADSP-21msp50 can be used as a memory-mapped peripheral to a host microcomputer (providing either 8- or 16-bit-wide transfers).

The host interface port can be thought of as an area of dual-ported memory, a set of “mailbox” registers that allow communication between the computational core of the ADSP-21msp50 and the host computer. The port's operation is completely asynchronous, allowing the host processor to write data into the HIP while the ADSP-21msp50 is operating at full speed.

The HIP can be configured for operation on an 8- or a 16-bit data bus—and for either a multiplexed address/data bus or separate address and data buses. Configuration is controlled via two mode pins, HMD0 and HMD1, and the HSIZE pin. Inputs to the HMD pins determine whether the address and data pins are separate or multiplexed. They also select the appropriate bus strobe pins: either individual read and write strobes, or a common read/write strobe pin. HSIZE configures the HIP for either an 8- or a 16-bit bus.

**On-Chip Converters:** The monolithic ADSP-21msp50 includes a complete analog front-end designed for high-performance voice band DSP applications. These converters (Figure 3)—known in telecommunications as linear codecs (COders/DECOders)—maintain wide dynamic range with superior SNR and THD, compared

to the use of quasi-logarithmic transfer functions in traditional A-law and  $\mu$ -law codecs.

The 16-bit-resolution ADCs produce samples at 8 ksps, with 65-dB SNR and THD (approximately 11-bit accuracy), commensurate with the needs of telecommunication and data communications; the 16-bit DAC updates at the same rate as the ADCs. Internal programmable-gain amplifiers, plus anti-aliasing and anti-imaging filters (for the ADCs and DAC respectively), minimize external components, system complexity, and cost.

The ADSP-21msp50 uses a sigma-delta conversion architecture, designed for a process similar to that used for the ADSP-2101. The gain of each of the two signal inputs can be adjusted from -12 dB to +26 dB via external gain-setting resistors. For each input, a first-order anti-aliasing filter (using an external capacitor) is adequate. The selected input, chosen by the internal multiplexer, reaches the sigma-delta modulator either directly or through an optional 20-dB gain stage. The nominal input span is  $\pm 2.5$  V.

The sigma-delta modulator produces 1-bit samples at a 1.0-MHz rate. This serial bit stream is operated on by a digital anti-aliasing low-pass filter and a high-pass filter to produce a 16-bit signal at an effective 8-kHz sampling rate ( $125\times$  oversampling). This 16-bit signal is then available for processing by the ADSP-21msp50's DSP core.

For analog *output*, signals sent from the DSP core to the DAC are first high-pass filtered, and then low-pass filtered to produce 16-bit samples at a 1.0-MHz rate. The digital sigma-delta modulator noise-shapes the data stream and reduces the sample width to one bit. This data stream is fed to a one-bit DAC, and its output is easily smoothed by an analog filter. The output of the analog filter is fed to the output amplifier, which has a  $\pm 2.5$ -volt range.

**Power-Saving Modes:** The ADSP-21msp50 has two power-saving features. These can be critical in many power-sensitive applications, such as battery-operated equipment.

First, the *IDLE* instruction, also used on the ADSP-2101, when executed, puts the processor into a low-power standby state. In this state, most of its circuitry is disabled, except for the host interface port, serial ports, timer, clock, and interrupt logic; full operation is not resumed until an external Interrupt occurs and is

serviced. A *power-down mode*, externally initiated by the *PWD* pin, puts the device in an extremely low-power mode. Within the *PWD* mode are separate, localized power-down features for the converter's analog and digital subsections; the mode is controlled by bits in the memory-mapped converter-control register.

## DEVELOPMENT TOOLS

As with any microprocessor, a full line of development tools is required to provide designers with the support needed to quickly and easily design with the device. Like other members of the ADSP-2100 family, the ADSP-21msp50 is fully supported with both software and hardware tools.

Since the ADSP-21msp50 is code-compatible with earlier members of the family, all code already written for the ADSP-2100 and derivatives can be easily ported to it. In addition, specific cross-software tools—including a simulator, assembler, linker, and system builder—are provided for the ADSP-21msp50. A C compiler is also available for designers interested in high-level language support. These software tools are supported on IBM PC AT (and compatibles), VAX, and SUN platforms.

Analog Devices hardware tools for the ADSP-21msp50 include the EZ-LAB™ demonstration board, the EZ-ICE™ midrange in-circuit emulator, and a full-featured emulator with trace capability.

## APPLICATIONS

The ADSP-21msp50 is a voiceband mixed-signal processor for signals from dc to up to 4 kHz. The processor and its analog front end are well suited for any applications that interface to real-world signals in that frequency range. Present cellular phone technology transmits voice as an analog signal, while supervision and control between the phone and its base station are done digitally on a parallel channel. Digital mobile radio—DMR<sup>5,6</sup> (Figure 4) is an emerging application that can fully exploit the capabilities of the ADSP-21msp50.

<sup>5</sup>Vary, P., K. Hellwig, et al, "Speech Codec for the European Mobile Radio System." *IEEE ICASSP 1988 Proceedings*, page 277.

<sup>6</sup>Freeman, D.K., G. Cosier, et al, "The Voice Activity Detector for the Pan-European Digital Cellular Mobile Telephone Service." *IEEE ICASSP 1989 Proceedings*, page 369.

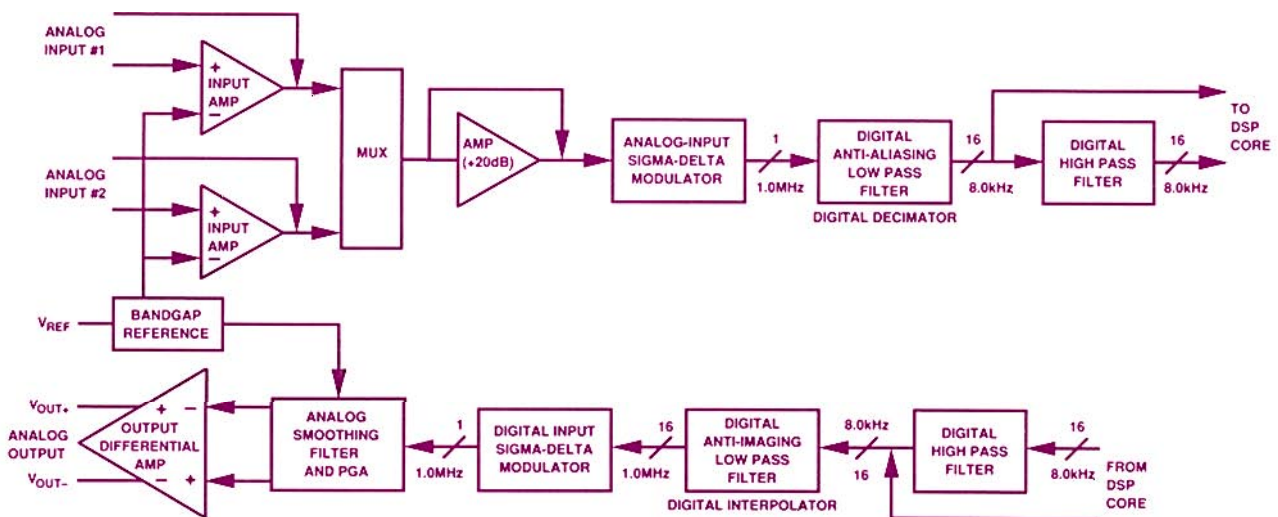


Figure 3. Block diagram of the ADSP-21msp50's analog channel.

There are several reasons why voice is being digitally encoded in mobile radio. In the United States, the popularity of cellular phones has resulted in saturation of the frequency spectrum in some of the country's largest metropolitan areas. Digital technology will allow the cellular phone system capacity to be tripled within the same spectrum allocation. In Europe, digital technology is being applied to support a common, unified European communication standard, which goes into effect by 1992. The goal is to offer standard mobile phone services so that a European mobile phone can be operated in any European country supporting the standard.

Although a directly digitized voice signal requires more bandwidth than an original analog voice signal of comparable fidelity, digitization permits the use of techniques that can significantly reduce transmitted bandwidth or increase capacity. In digital cellular phones, these techniques are data compression (and expansion) and discontinuous transmission (which increases spectrum-usage efficiency).

As a speech codec, the ADSP-21msp50's task is to *compress* digitized voice prior to transmission, and *expand* received voice signals. The compression techniques used are based on an enhanced version of linear predictive coding (LPC) algorithms with long-term Prediction (LTP). Regular pulse excitation (RPE) enhancements to the LPC algorithms are added to improve the quality of the encoded speech.

In the European implementation of the algorithm for speech compression/expansion, the voice signal is divided into a series of 20-ms segments (windows). Each window is sampled 160 times, with 13-bit resolution (the sampling rate is 8 ksps). The compression algorithm reduces the samples to 76 coefficients in each window (260 bits total) for an encoded bit rate of 13 kbps. Redundant bits are added by the processor for error detection and correction at the receiver, increasing the final encoded bit rate to 22.8 kbps. (The bits within one window, and their redundant bits, are interleaved and spread across several windows for robustness.)

The ADSP-21msp50 can also provide discontinuous transmission control. Discontinuous transmission allows the system to shut off during pauses between words. Besides reducing transmitter power consumption, this increases the system's call capacity by reducing the interference between channels, and allowing other users to

share the channel. It is estimated that this will approximately double the call capacity of the cellular system. In order to implement the discontinuous transmission function, the ADSP-21msp50 is called upon to perform several tasks including:

- *voice activity detection* to detect when speech is present—and when it is absent during pauses and gaps
- *comfort noise insertion* to synthesize artificial car noise, which eliminates the unpleasant effect of switching between speech (with audible car background noise) and silence between speech periods. This greatly increases the intelligibility of conversation (it also reassures the user that the cellular phone is indeed operating!)
- *output muting* when lost-speech frames are received.

The ADSP-21msp50 can perform all of the above tasks within the 20-ms sampling window because of its optimized DSP architecture and the special on-chip peripherals associated with it. The sigma-delta converters provide the necessary interface to the speaker and microphones. The parallel host interface port communicates with a host processor, which is responsible for loading the ADSP-21msp50 with the appropriate programs during power-up, dialing, and actual conversation phases of a complete call.

Benchmarks show that the speech encoding and decoding, and voice activity detection algorithms require just 25% of the DSP's time. The ADSP-21msp50 operates at a clock rate of 50 MHz. It is packaged in a 132-pin quad flat pack and priced at \$30 (100,000s).

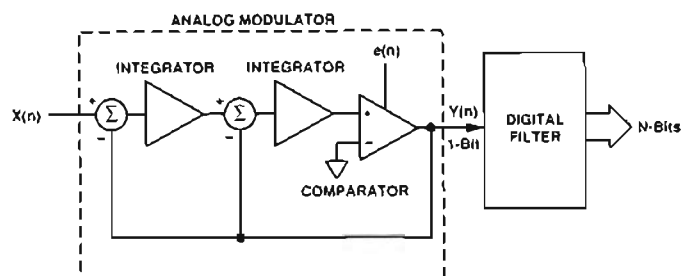


Figure 5. Sigma-delta analog modulator.

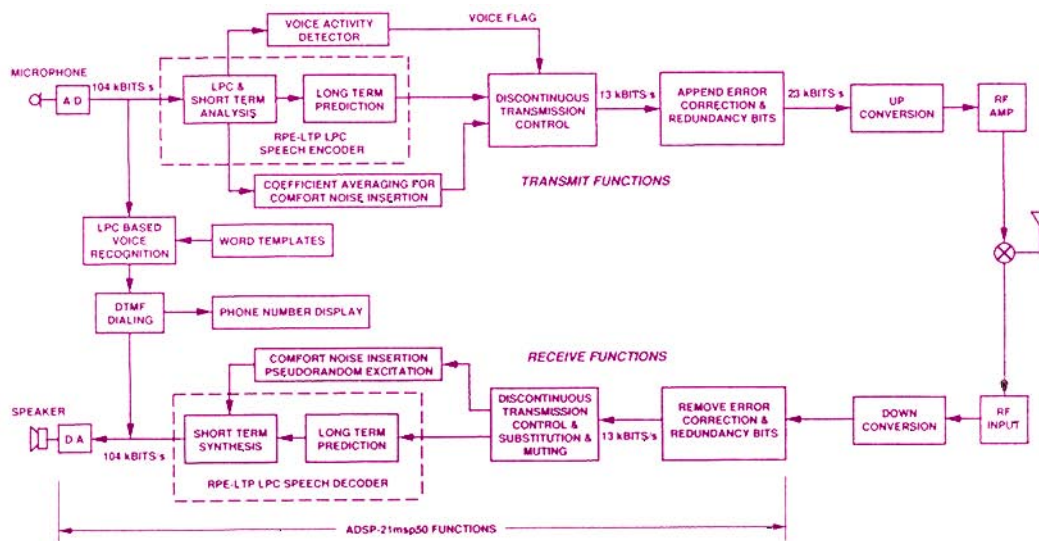


Figure 4. Digital cellular phone.

Sigma-delta a/d conversion architectures are well-suited to digital IC process design and fabrication. Unlike a traditional converter, which uses precision elements (often laser-trimmed) to maintain resolution and accuracy, the sigma-delta-modulation architecture produces conversions with just one bit of resolution at very high sampling rates, i.e., *oversampling* (sampling at a rate many times the Nyquist rate); it is followed by digital filtering and *decimation* to produce output digital values with higher resolution at a slower rate. Sample-holds are unneeded, because the aperture uncertainty can be quite small, since it depends only on the one-bit sampling rate, which is usually in the MHz region.

Of the overall sigma-delta conversion circuitry, a significant fraction is purely digital and inherently less noise-sensitive than precision analog circuitry. In addition, noise can be further reduced by a digital filtering process. In IC layout and fabrication, the digital circuitry of the converter subsection uses the same design techniques as the rest of the digital chip—just more digital logic.

The sigma-delta converter, unlike traditional converters, *manages* the conversion noise: the oversampling techniques and digital filtering move most of the quantization noise outside of the frequency band of the signal. This permits accurate conversion in the desired band but provides no useful information for frequencies falling outside the specified bandwidth. A sigma-delta converter has narrower bandwidth than a successive-approximations converter but typically wider bandwidth than a dual-slope type.

**Sigma-Delta Modulator:** The first part of the converter is the sigma-delta analog modulator, which converts an input signal into a 1-bit high-rate data stream. The narrow-band (e.g. 4-kHz bandwidth) input signal,  $X(n)$ , is transformed into a continuous serial stream of 1's and 0's, at a rate (e.g., 1 MHz) determined by the modulator clock. Since the modulator output of the sigma-delta converter has just one bit of resolution, a large number of samples need to be averaged (by digital filtering) to convert the input signal to a high-resolution, low-rate result.

The analog modulator (Figure 5) represents a second-order filter. The integrators behave like low-pass filters (for signal), and the comparator output generates a single bit containing the associated quantization error. Each integrator can be represented in the frequency domain with a filter amplitude response of  $1/f$  or, in the  $z$  domain,  $z^{-1}/(1 - z^{-1})$ . The error term,  $e(n)$ , in the comparator represents quantization noise as the integrated signal is converted to a digital value (0 or 1).

Since the chopper-like action of the clocked, latched comparator converts the signal to a high-frequency ac, varying about the average value of the input, the effective quantization noise at low frequencies is greatly reduced (to quantization noise, the integrator loop looks like a high-pass filter). The exact nature of the resulting noise depends on the chopper rate, the integrator time constants, and the precise span of the voltage fed back. These characteristics determine the bandpass limits for the sigma-delta converter.

**Digital Filter:** The second half of the sigma-delta converter is the digital filter. Once noise has been shaped to occur mostly outside the band of interest, a digital filter is used to low-pass filter the signal, effectively removing the unwanted high-frequency components. The oversampled (e.g. 1-MHz) bit stream is fed into the digital filter and decimated into a more manageable signal bandwidth (e.g., 8 kHz), but with much higher resolution (16 bits in this case).

## Sigma-Delta Converters and Noise

In a traditional converter, the quantization noise is randomly distributed (white noise). Low-pass filtering, needed for anti-aliasing at the front end, eliminates only the noise outside the passband; noise within the passband is unaffected. The effective number of bits,  $n$ , in the conversion can be determined from:

$$(\text{SNR [dB]} - 1.78)/6.02 = n \text{ effective bits}$$

Here is where one of the major differences between the sigma-delta and conventional converters is seen. If the quantization noise could actually be shaped so that the greatest part of its overall spectrum occurs at frequencies above the signal spectrum, there would be very little noise in the signal band of interest. Also, the noise in the out-of-band area could be filtered without affecting the input signal spectrum. The number of effective bits would depend principally on the degree of oversampling and the filter design.

Noise shaping is a consequence of the sigma-delta oversampling process. From the frequency-domain perspective, the integrator loop acts like an analog filter with low-pass characteristics for the signal and high-pass characteristics for the noise. Figures 6a through 6d show the effects of noise shaping and low-pass filtering for a signal at  $f_0$  with sampling at  $f_s \gg f_0$ . In the frequency band of interest, the 1-bit stream will accurately produce an  $n$ -bit input signal representation through appropriate filtering.

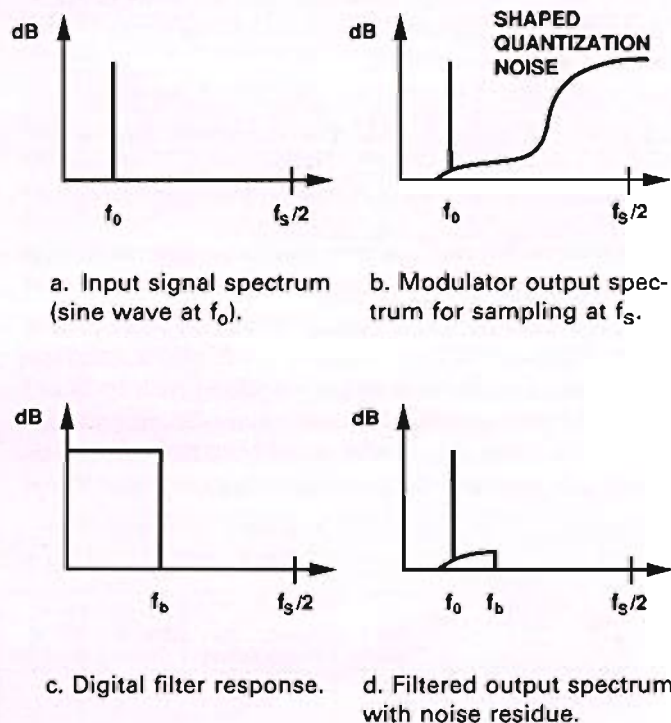


Figure 6. Sigma-delta-converter frequency response.

*The ADSP-21msp50 was designed at Analog Devices' Digital Signal-Processing Division, Norwood, Massachusetts, by teams headed by Greg Koker and Jim Wilson; members of the teams include Doug Hester, Steve Tsang, Kent Townley, Mark Diamondstein, and Gordon Cheung—all from DSP—and Paschal Minogue, of the ADBV Division, Limerick, Ireland.* ▶

# LOW-DISSIPATION MULTIPLE LINE DRIVERS/RECEIVERS

AD230-AD241 CMOS RS-232 device series use +5-volt supplies

AD401 & AD402 BiCMOS devices support RS-232 and RS-422

by Bill Schweber

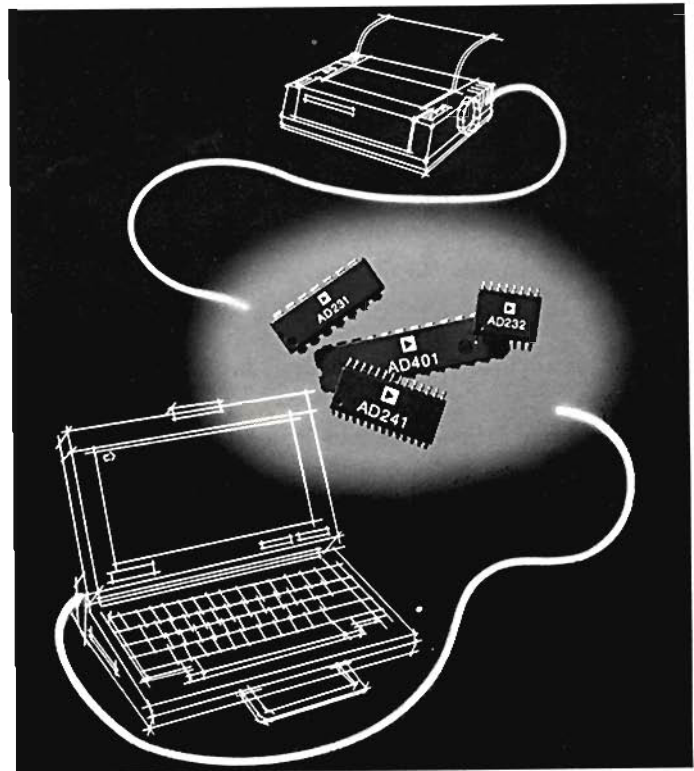
Two new series of integrated circuits, designated AD230 through AD241,\* and AD401 & AD402,\* provide the signal-level translation, drive capability, and receiver thresholds required in RS-232 and RS-422 interface applications. In addition, they make available such features as operation from a single +5-V supply (while delivering a bipolar signal output), multiple drivers/receivers in one package, low-power "shutdown" mode, TTL- and CMOS-compatible transmitter inputs/receiver outputs, and 3-state receiver output.

These line drivers and receivers are the interface between the outside world and the internal logic of an entity that must communicate using the key industry standards (RS-232 and RS-422) for interface voltage, timing, and related specifications.<sup>1</sup> The standards were established long before the existence and proliferation of complex battery-powered systems, such as laptop computers; but they are still among the most common physical interface specifications in use. System protocol, formats, and networking have become much more complex; nevertheless these basic standards define the signal appearance and driver/receiver performance at the interface where the unipolar logic signals (often 0 V and +5 V) within the system meet the reality of external signal cables and the non-digital world [see the sidebar: "The RS-232 and RS-422 Standards"].

Though transparent to the user's communication software and functionality, the drivers provide protection against many of the hazards that occur when extending electronic signals beyond the benign environment of a circuit board: overvoltage, misconnection, and power-up, -down, and -off conditions.

## THE AD230, AD231, . . . AD241

The AD230-through-AD241 family comprises 11 devices (Table 1). This series is used exclusively for RS-232 interfacing, especially in applications where only a +5-volt supply is available. The devices differ in number of drivers and receivers per package, as shown in the table. The AD230, AD235, AD236, and AD241 have externally controlled shutdown modes that can reduce power



dissipation to less than 5  $\mu$ W, ideal for battery-powered equipment.

The circuitry within these devices has three aspects: a charge-pump *voltage converter*, *receivers* (RS-232 to TTL/CMOS, including level shifters), and *transmitters* (TTL/CMOS to RS-232, also with level shifters). The RS-232 standard requires that transmitters provide at least  $\pm 5$ -volt output under defined conditions; receivers must accept as *valid* levels down to  $\pm 3$  V.

**Charge-pump voltage converter:** With the exception of the AD231 and AD239, all devices in the family include a *two-stage* charge-pump voltage converter; it converts the +5 volts from a

Table 1. AD230 through AD241: performance summary.

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown	TTL Three-State $\overline{EN}$	No. of Pins
AD230	+5 V	5	0	4	Yes	No	20
AD231	+5 V & +7.5 V to 13.2V	2	2	2	No	No	14
AD232	+5 V	2	2	4	No	No	16
AD233	+5 V	2	2	None	No	No	20
AD234	+5 V	4	0	4	No	No	16
AD235	+5 V	5	5	None	Yes	Yes	24
AD236	+5 V	4	3	4	Yes	Yes	24
AD237	+5 V	5	3	4	No	No	24
AD238	+5 V	4	4	4	No	No	24
AD239	+5 V & +12 V	3	5	2	No	Yes	24
AD241	+5 V	4	5	4	Yes	Yes	28

<sup>1</sup>Schweber, W. L., *Data Communications*. NY: McGraw-Hill, 1988.

\*Use the reply card for technical data.



single supply to the bipolar higher voltage levels ( $\pm 10\text{ V}$  in this instance) needed for RS-232 operation (Figure 1). The first stage doubles the 5-volt level to 10 volts; in the second stage, the 10-V level is inverted to provide  $-10\text{ volts}$ . The AD231 and AD239, already specified for a 12-volt supply, need only a single-stage charge-pump voltage converter—as an inverter—to develop  $-12\text{ V}$ .

In Figure 1's first diagram (the voltage doubler), switches S1, S2 are closed while S3, S4 are opened, and vice versa. During the first half-cycle of the oscillator, C1 is charged to  $+V_{CC}$ ; during the second half-cycle, C1 charges C3; after many cycles, the voltage across C3 is almost equal to  $V_{CC}$ , but isolated from it by the break-before-make switches. This permits the lower end of the output to be connected to  $V_{CC}$ , whereupon the voltage between the upper end and GND will be  $2V_{CC}$ . When current drawn by a load tends to draw C3's voltage down, it will be refreshed by C1 on each cycle. The voltage inverter works in the same way, reproducing its input voltage ( $V^+$ ) between the output terminals; then, when the upper output terminal is connected to GND, the lower output terminal will be at  $-V^+$ .

The capacitors are normally connected externally; however, AD233 and AD235 provide internal capacitors in the final package for applications where space is critical.

**Transmitter:** The transmitter section consists of the drivers; they provide level-conversion and suitable drive current. With  $V_{CC}$  of  $+5\text{ V}$  and typical RS-232 load, the output swing is  $\pm 9\text{ V}$ , well above the  $\pm 5\text{-V}$  minimum requirement of RS-232. The driver output slew rate is limited to  $30\text{ V}/\mu\text{s}$  (as required by the standard) without any external slew-rate limiting capacitors. In the power-off state, output impedance is greater than 300 ohms.

**Receiver:** The receivers, complementary to the drivers, have level shifters that accept inputs of  $\pm 3\text{ volts}$  (or more) and provide TTL/CMOS output levels. The receiver inputs, protected for up to  $\pm 30\text{ volts}$ , use Schmitt trigger circuits with 0.5-volt hysteresis to minimize errors caused by input signals that are noisy or have slow transitions.

**Shutdown and Enable:** To conserve power, the AD230, AD235, AD236, and AD241 have a separate control input that can disable the device, reducing current consumption from the nominal  $5\text{ mA}$  to less than  $1\text{ }\mu\text{A}$ . When this input is low, the charge pump is disabled, receiver inputs go to high impedance, and the driver outputs are turned off.

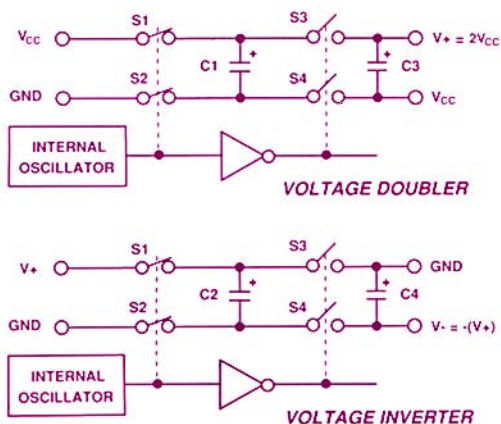


Figure 1. Two charge-pump voltage converter stages.

The AD235, AD236, AD239, and AD241 have an *enable* input used to set the receiver output state to either active or high-impedance mode, as seen by the rest of the system circuitry. This allows the device outputs to avoid bus conflicts when connected to a microprocessor data bus and permits receivers from different devices to share a common data line.

### The AD401 and AD402

For applications where RS-422 is used instead of—or in addition to—RS-232, the BiCMOS AD401 and AD402 line drivers/receivers provide the interface between TTL signal levels and the prescribed levels of the standards. Both parts can be configured, via two *select* pins, to be compatible with either the single-ended RS-232 standard or the differential RS-422 standard. The *select* pins' two-bit code permits four different choices of RS-232 and/or RS-422 drivers and receivers (Figure 2). Both devices require  $+5$  and  $\pm 12\text{ V}$  supplies.

The AD401 and AD402 have a very useful test feature called the *loopback* mode. When it is invoked, by setting the loopback pin at the IC's logic *low*, two actions result:

- the external driver outputs are switched to their high-impedance mode, and
- they are internally switched to their respective receiver inputs. This internal switching thus provides a non-inverting path from the driver TTL inputs to the receiver TTL outputs. The system can then perform a thorough self-test of all aspects of its internal transmit/receive channel (including the interface with the driver and the receiver but not the external physical connector and channel link) at speeds up to 3,000 baud.

The AD401 and AD402's RS422 drivers and receivers are specified to a maximum of 500 kilobaud. To eliminate response to high-frequency noise pulses, the receiver circuitry includes filtering to ignore input pulses less than  $1\text{ }\mu\text{s}$  in width. Like the devices described earlier, the AD401/402's RS-232 receivers use hysteresis to minimize spurious outputs resulting from low-amplitude noise during slower-speed signal transitions.

The AD230 through AD241 are available in a wide selection of packages, ranging from 14-pin plastic DIPs to 28-lead SOICs. The AD401 and AD402 are housed in 24-pin plastic and ceramic DIPs. Prices (100s) in the lowest-cost package range from \$2.70 for the AD232 to \$4.54 for the AD241; and \$9 for the AD401 & AD402.

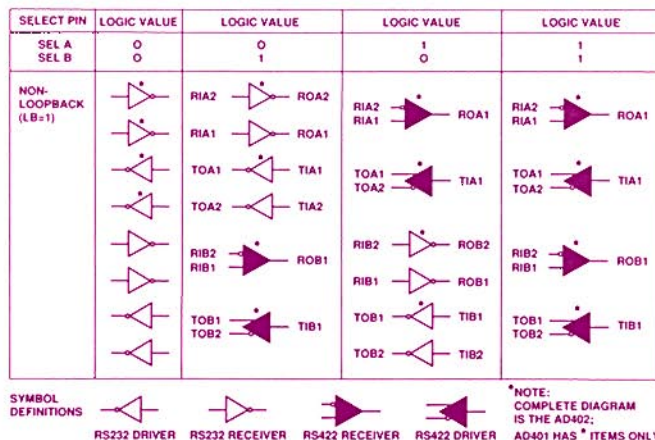


Figure 2. Selectable configurations of the AD401 and AD402.

## THE RS-232 AND RS-422 STANDARDS

Standards are essential in communications systems to ensure that both parties speak a common language at all levels and thus can both properly *receive* messages and *understand* them. A given communication standard may define *protocols*, *formats*, and/or the *physical interface*.

- *Protocol* defines the rules of conversation: which party speaks, when, how to respond, how to act when abnormal conditions occur.

- Below the level of protocol, *format* specifies how the overall message is built up: number of bits and placement of user data, how data is represented, message opening- ("preamble") and closing fields, error-correction bits, and similar factors.

- On the next level is the *physical interface*, which specifies the bit timing, signal levels, and role of the physical lines in the data link.

The RS-232 standard (now in Revision D), promulgated within the United States by the Electronic Industries Association (EIA), defines some aspects of this last—the physical interface. (There are comparable international standards.) It specifies *single-ended* signal transmission over a link between a single source and a single receiver, with a binary "0" represented—at the source—by any voltage from +5 to +25 V and a "1" represented by a voltage from -5 to -25 V. At the receiver, a "0" is any voltage greater than +3 V, and a "1" is a voltage less than -3 V.

In addition, RS-232 allows transmission at rates up to 20,000 baud, and guarantees performance at a specified maximum load capacitance for distances up to 50 feet (although the standard is often used for less-than-maximum rates, lower load capacitances, and longer distances). Finally, the standard defines the electrical abuse that the RS-232 drivers and receivers must withstand, with power on and off, the maximum allowable signal slew rate and the minimum time in the transition region.

The single-ended signals of RS-232 share a common ground with each other and with the system ground (Figure 3). Although this saves wiring, it introduces noise and common-mode signal problems. The relatively wide span signal swing specified—needed to avoid noise-induced errors—also precludes high-speed operation because of the limit on slew rate and demands on the drivers.

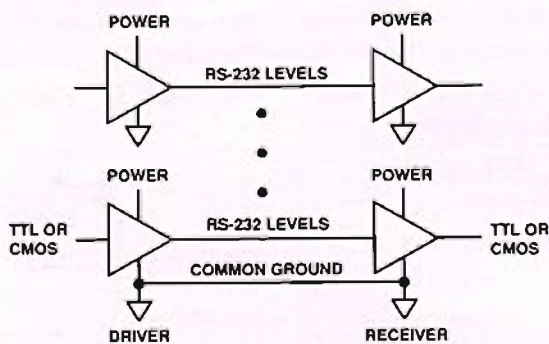


Figure 3. RS-232 single-ended configuration.

To overcome the limitations of RS-232, the EIA developed RS-422, a *differential* standard with a different set of signal levels and thresholds. RS-422 provides for systems with two leads per data link (Figure 4) and operation at up to 10 megabaud.

The source drive must provide at least +2 to +6 V and -2 to -6 V for binary "0" and "1", respectively, while the receiver thresholds for valid data bits are +200 mV for "0" and -200 mV for "1". This reduces the slew rate demands on the driver circuitry, (compared to much wider signal swings) and allows more cable capacitance for a given baud rate. The RS-422 standard allows one driver and *up to ten receivers* on the link, with a total length up to 4,000 feet (maximum data rate and maximum distance are not available simultaneously; the standard provides a chart to define the relationship.)

The reader should note that none of these standards defines how the data itself must be represented; that requires a *format*-level standard. ASCII (American national Standard Code for Information Interchange) is most common, using 7 or 8 bits/character; an extra parity bit is often appended as well. However, some applications use non-ASCII codes or simple binary.

There are good reasons to combine RS-232 and RS-422 standards (and therefore both types of drivers and receivers) in one system—and the AD401 and AD402 are designed for such systems. Often, the two data paths (one for transmit, one for receive) also require several control (handshake) lines to properly manage the link protocol. These control lines include Request to Send, Clear to Send, Data Set Ready, and Data Terminal Ready, (but many applications do not need all four lines).

If RS-422 is used throughout, many signal wires (and a large connector) are required, at substantial cost. In practice, however, the control lines operate at much slower rates than the data lines, since their transitions are much less frequent. Control-line activity depends on the amount of data buffering within the source and receiver, how often the buffer is serviced, the overall amount of data being sent, and many other system-level factors. Typically, the control lines have one-tenth or less the amount of activity that the data lines have.

Accordingly, it is practical to use the differential RS-422 standard for the higher-rate data and the single-ended RS-232 standard for the control lines in many cases. The result is a significant saving in cable and connectors. ▶

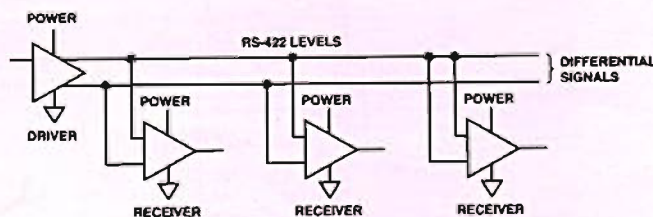


Figure 4. RS-422 differential configuration.

# PEAK DETECTOR CIRCUIT CAPTURES 200-ns PULSES

With speed and low droop—other performance enhancements feasible

Key is FET-input op amp fabricated on complementary-bipolar process

by Lew Counts and Mark Murphy

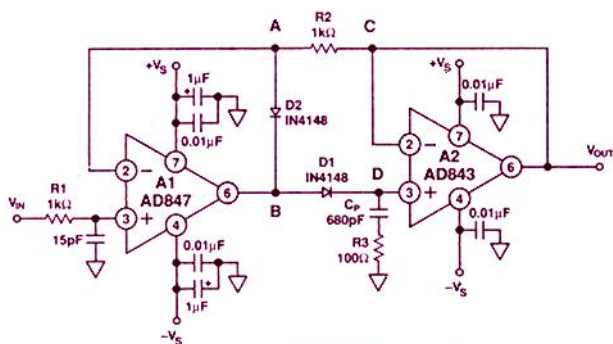
The classic peak-detector architecture (Figure 1) achieves high speed with the Analog Devices AD847\* and FET-input AD843\* op amps, fabricated on ADI's complementary-bipolar (CB) process (*Analog Dialogue* 22-2). Both settle fast and stably, with high slew-rate and wide bandwidth—critical for acquiring fast peaks. And the AD843's FET input promises a low droop rate.

This circuit captures the most-positive value of an input waveform; it accurately captures the peak value of pulses as narrow as 200 ns and has a droop rate of  $\leq 20$  mV/ $\mu$ s. Such speeds have been difficult to achieve because conventional FET-input op amps have poor performance as followers; slow to track fast-changing inputs, they overshoot severely on catching up, then settle slowly.

## OPERATION

A peak-detector is a sample-and-hold. In the *sample* mode, it follows the input when it rises above a previously held voltage. When the input starts decreasing, the circuit goes into *hold*; its output remains (ideally) constant at the highest value tracked. It can be reset for a new run by momentarily discharging its capacitor.

Amplifier A1 and diode D2 form a unity-gain buffer follower except when transiently supplying the current required to charge the hold capacitor in the sample mode. FET-input A2 is a unity-gain buffer for the hold capacitor; its output drives a current through R1 and D1 proportional to the difference between the held value and the input. When the input signal seeks to rise above a previously stored value, A1 senses the sign change and quickly responds with a transient positive output swing that charges the holding capacitor  $C_p$  to catch the input signal. Amplifier A2 must respond very quickly to keep the voltage at point C following the voltage at point A; else the current through R2 will seek to reverse, which would cause a very large—and troublesome—positive swing at A1's output.



TYPICAL BEHAVIOR IN BOTH MODES

	$V_{in}$	$V_A$	$V_B$	$V_D$	$V_C = V_{out}$
AT $t_1$ , HOLDING 7V	4V	4V	4V - DIODE	7V	7V
AT $t_2$ , HOLDING 7V	6.9V	6.9V	6.9V - DIODE	7V	7V
AT $t_3$ , TRACKING	7.1V	7.1V	7.1*	7.1V	7.1V

\* $>7.1V$  WHILE ACQUIRING NEW VALUE

Figure 1. Schematic diagram of peak-detector circuit.

\*Use the reply card for technical data.

When the signal decreases again, A must follow the input, so the output of A1 swings in the negative direction, one diode drop below A, keeping D1 turned off. The  $< 1$  nA of the FET-input amplifier ensures that the capacitor's droop rate depends only on the reverse leakage current of D1 ( $< 10$  nA here). The 200-V/ $\mu$ s slew rate of A2 is significantly higher than the rate at which A1 charges the hold capacitor, lessening the delay in the feedback path through A2 to point A. Offset and gain errors of A2 are nullified because, in *sample*, the input of A2 is driven at the correct value for the output to track the input; and this value is retained during Hold.

## PERFORMANCE

Figures 2 and 3 show two key performance measures. Figure 2 shows the rising input and capture response for an 8-V pulse. Amplifier A1 charges the 680-pF hold capacitor fast enough to swing from the previously held 5 volts to attain (and overshoot) the 8-volt peak in 100 ns, settling to a new value in 250 ns. Figure 3 shows the circuit's droop during Hold; the output (top trace) decays from an 8-volt peak by approximately 1 V in 75 ms.

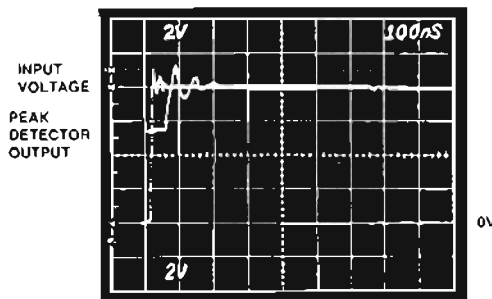


Figure 2. Peak capture demonstration, showing fast input pulse. Peak detector response visibly settles within 250 ns.

The peak detector can be speeded with decreased  $C_p$ , at the expense of increased overshoot and droop. Conversely, increasing  $C_p$  will reduce the droop rate but increase the detector's response time.

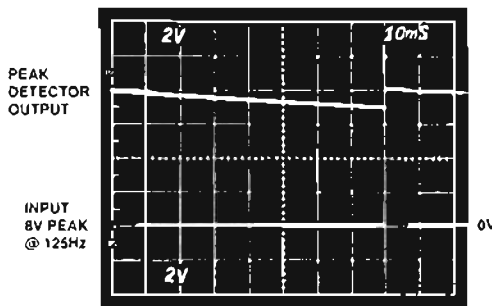


Figure 3. Long-term peak-detector output showing droop (upper), input waveform (lower).

## ENHANCEMENTS

To detect negative peaks (*valleys*), reverse the diode polarities. If a single peak-follower droops too much, two peak detectors can be cascaded—the first for speed, the second for low droop. For “infinite hold”, cascade an ADC and DAC after the peak detector. ▶

# MEASURING AMPLIFIER DIFFERENTIAL GAIN & PHASE ACCURATELY

## Video systems require 0.1% gain and 0.1° phase differences

### Valid measurements need proper instrumentation and techniques

by Scott Wurcer and Jeff Smith

In standard television systems, color (chrominance) information is conveyed by a phase- and amplitude-modulated subcarrier. The NTSC (National Television Standards Committee—see sidebar) system used in the US and Japan employs a 3.58- (actually 3.579545-) MHz color subcarrier, while the United Kingdom's PAL system and France's SECAM system use a 4.40-MHz subcarrier.<sup>1</sup>

Since amplitude and phase carry color information, if the circuitry of the signal path causes any modulation or variation of these quantities in the subcarrier or its sidebands, the viewer will see a color change. Because of this, video systems have stringent requirements for linear behavior, as commonly defined in terms of two error quantities: *differential gain* and *differential phase*.

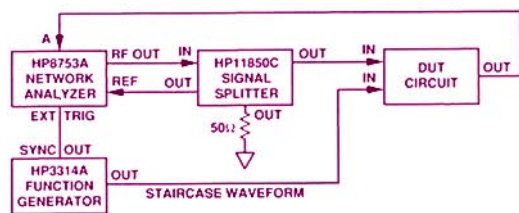


Figure 1. The test setup for differential gain and phase uses a network analyzer to supply a 3.58-MHz subcarrier for chrominance and a staircase generator to simulate an NTSC staircase test signal for luminance.

*Differential gain* defines the change in output *amplitude* of a small high-frequency sine wave (i.e., the subcarrier) at two stated levels of a low-frequency signal on which it is superimposed, and *differential phase* defines the change in output *phase* under the same conditions. System differential gain of less than 0.1% and differential phase of less than 0.1° are usually required for acceptable overall performance.

These system specifications mandate even more stringent standards for individual circuit components. Typical goals for op amps used for handling video signals in system designs are currently 0.02% and 0.05° (and will be more like 0.01% and 0.01° in

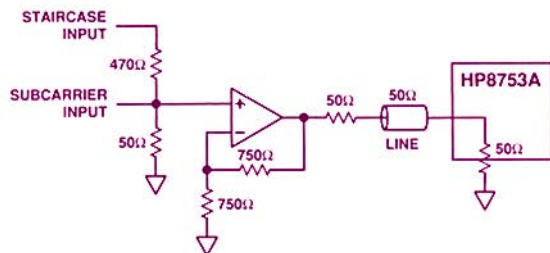


Figure 2. The DUT circuit uses a gain-of-2 amplifier to drive a 50-Ω double-terminated load. The outputs of the network analyzer and the staircase generator, summed at the input, create the composite video test signal.

<sup>1</sup>For more background, see "Characterizing and Testing A/D and D/A Converters for Color Video Applications," by Walter A. Kester, IEEE Transactions on Circuits & Systems, vol. CAS-25, no. 7, July, 1978, pp. 539-550.

the HDTV era). Measurements at these levels exceed the resolution of normal video test equipment, which typically has specs of the same order as the NTSC/SECAM system-level specs of 0.1% differential gain and 0.1° differential phase.

### A TEST SETUP WITH IMPROVED RESOLUTION

Figure 1 shows a high-resolution test setup that uses an arbitrary waveform generator (HP3314A) and a network analyzer (HP8753A) to measure differential gain and phase with accuracies of 0.01% and 0.01°. The arbitrary waveform generator produces the level changes called for in the error definitions by a staircase or ramp waveform that simulates the luminance (picture brightness) aspect of the video waveform.

The network analyzer supplies the color subcarrier waveform (at 3.58 MHz, for example) and measures the differences in the color subcarrier's gain and phase by comparing the output of the device under test (DUT) with the reference signal returned by the signal splitter (HP11850C).

Quasi-static gain and phase tests, in which a series of dc voltage steps are individually superimposed on the color subcarrier signal, do not always yield correct results because the DUT characteristics can change with device temperature. Even if ambient temperature is held constant, the device temperature changes in real time because the DUT's power dissipation, which is strongly dependent on its average dc output current, changes as the stepped input causes step changes in the output.

Thus, in some amplifiers, the differential gain and phase measurement drifts visibly as the amplifier's temperature changes after a sudden change in the dc level of an input signal. The technique discussed here repetitively superimposes a rapidly changing dynamic signal on the subcarrier, thus more closely approximating a true NTSC differential-gain and -phase test.

The DUT circuit, Figure 2, shows an op amp connected in the most common video configuration as a gain-of-2 amplifier driving a 50-Ω double-terminated (also known as *reverse-terminated*) line. The 50-Ω termination resistor at the op amp output presents the proper impedance to the transmission line for reflections, and thus absorbs them. The gain of two is needed for overall unity gain, because the 50-ohm forward termination resistor and the 50-ohm load at the op amp output form a gain-of-one-half voltage divider.

The 3.58-MHz color subcarrier and the staircase (luminance) signal are summed at the input to the op amp. This summing superimposes the staircase on the color subcarrier, thus generating the pseudo-standard video test waveform. The differential gain (or phase) is defined as the maximum difference in gain (or phase) of the subcarrier caused by any two steps in the staircase waveform.

Typical sets of test results are shown in Figures 3 and 4; each division of the horizontal scale (proportional to time) is a step of the modulating staircase, while the vertical scale shows the relative difference in gain or phase. Figure 3 shows the performance

of an Analog Devices AD844; the vertical scales are 0.005% and 0.01° per division, while the staircase span is from 0 to 643 mV (i.e., 0 to 90 IRE). These measurements indicate peak errors of 0.008% for differential gain and 0.025° for differential phase. Figure 4 shows comparable results for an Analog Devices AD845, with scales of 0.02% and 0.01° per division. Differential gain is 0.05%, with differential phase of 0.023°.

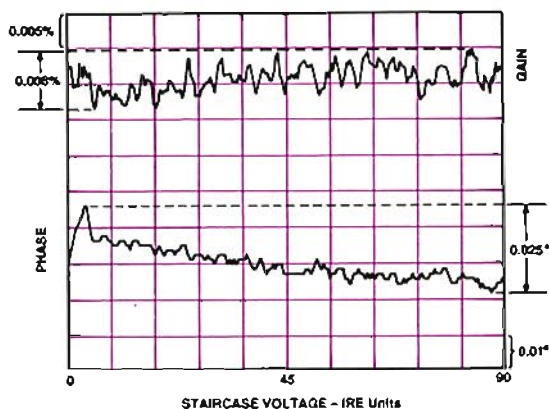


Figure 3. Differential gain and phase of the AD844 vs. staircase voltage.

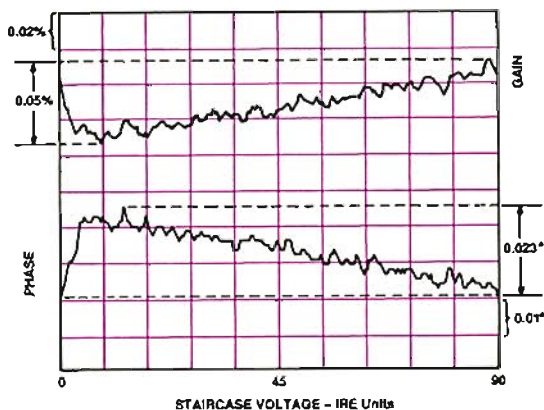


Figure 4. Differential gain and phase of the AD845 vs. staircase voltage.

The authors would like to thank Bob Clarke for his assistance in the preparation of this article.

### COLOR VIDEO INFORMATION ENCODING

The color video signal captured by a TV camera comprises the three primary additive colors, which are separated by passing the image through color filters. The signal-processing challenge is to encode these three distinct analog signals into a single signal for transmission over a single channel.

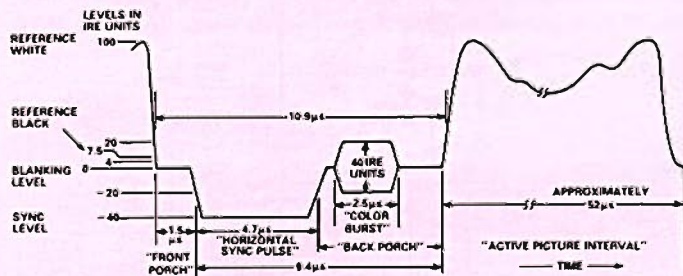


Figure 5. TV signal, amplitude versus time format.

<sup>2</sup>The standard was originally developed under the aegis of the Institute of Radio Engineers (IRE, later merged with the American Institute of Electrical Engineers to form the IEEE).

The challenge is intensified by the need for compatibility with conventional “black and white” systems: the color-encoded signal must appear as an appropriate grey-scale signal in a monochrome system, and a monochrome signal must be faithfully rendered in shades of grey when displayed on a color system. As a further constraint, color video bandwidth is limited to the original 6-MHz allocation.

The TV standard (EIA RS-170) for encoding of monochrome video is built on the elements of a composite signal repeated for each horizontal scan interval; the amplitude variations are grouped into intervals for vertical synchronization, horizontal synchronization, blanking during retrace, and the actual video intensity signal (the vertical scale for this composite signal is graduated in IRE units<sup>2</sup> (0 to 100), Figure 5).

Color transmission uses amplitude and phase information to encode the color signal compatibly. Eight cycles of color subcarrier, transmitted as a color burst on the “back porch” between the horizontal sync pulse and the actual video signal, are used by the receiver as a reference when demodulating the phase information.

The red/green/blue (RGB) color information is encoded by the following scheme: A luminance (brightness) signal is produced by combining the R, G, and B signals through a resistor matrix in weighted proportion. The coefficients of this weighting are chosen, using color-perception data, to produce what appears to the human eye to be a correct intensity (gray-scale) level.

In addition, two other combinations of R, G, and B are developed; they are called the chrominance (chroma) signals, since they convey the actual color information. Different weightings are used to produce an in-phase signal (I) and a quadrature signal (Q); they modulate the color subcarrier via a balanced modulator, yielding two sidebands—with the carrier suppressed.

Since the eye is more sensitive to detail in colors represented by the I signal (weighted toward yellow-red through greenish-blue), the in-phase I signal is designed to have wider bandwidth than the quadrature Q signal—which is weighted towards reddish-blue to yellowish green. The bandwidth allocations within the frequency spectrum of the baseband color signal are shown in Figure 6.

The color receiver uses the received color burst to phase-lock its internal reference to the missing color subcarrier, and then demodulate the I and Q signals. When a monochrome receiver acquires the signal, it simply uses the luminance signal to produce gray-scale, ignoring the I and Q signals entirely. In color reception, any gain- or phase inaccuracy of the color signal causes distortion and error in the demodulation process, resulting in unpleasant and generally unacceptable color shifts. The viewer can manually adjust the receiver to remove these shifts but would consider it an unnecessary inconvenience.

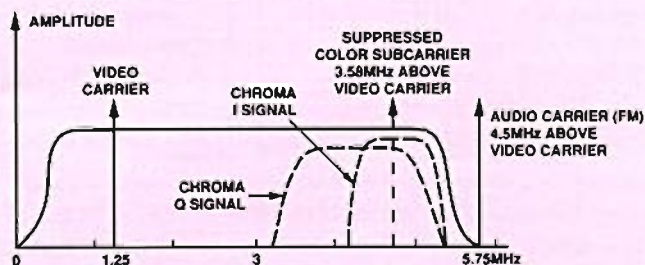


Figure 6. Baseband color TV signal spectrum.

# 3/4-GHz MONOLITHIC UNITY-GAIN BUFFER FOR ANALOG SIGNALS

AD9630 has low distortion, low output impedance, excellent linearity, fast settling

Use it to drive the input impedance of flash a/d converters

The AD9630\* is a monolithic unity-gain buffer with very wide bandwidth. It is useful for impedance transformation in wideband analog circuits where low output impedance is necessary—for example, in driving the nonlinear input impedance of flash converters.

Unlike many high-speed buffer circuits, which are open-loop, the AD9630 employs closed-loop design techniques (patent pending) to achieve excellent gain accuracy, wide bandwidth, and low distortion. For example, minimum gain over temperature is 0.98 V/V, and typically 0.99, for a 2-volt p-p swing; -3-dB bandwidth is typically 750 MHz small-signal (330 MHz minimum over temperature), and 120 MHz large-signal (70 MHz min over temperature). Small-signal gain and phase response are plotted in Figure 1.

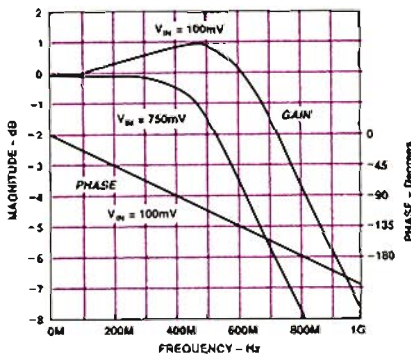


Figure 1. Forward gain and phase response.

The AD9630 slews at 1,200 V/ $\mu$ s, with maximum rise/fall time (over temperature) of 1.6 ns for 1-volt steps and 6.1 ns for 5-volt steps (Figure 2). Group delay is only 0.7 ns, and phase deviation from linear is only 0.7° for frequencies from dc to 150 MHz. Two-volt steps settle to  $\pm 0.1\%$  in 5 ns (12 ns max over full temperature, 8 ns max for  $T \leq 25^\circ\text{C}$ ) and to 0.02% in 8 ns typical (18 and 13 ns max at high and low temperatures). Differential gain and phase are 0.015% and 0.025°.

For 2-volt p-p sinewave signals, maximum 2nd-harmonic distortion at 4.3 MHz, 20 MHz, and 60 MHz is respectively -74, -59, and -43 dBc (-80, -66, and -52 dBc typical); comparable figures for third harmonic are: -79, -68, and -40 dBc max and

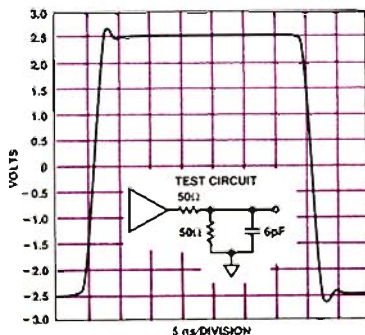
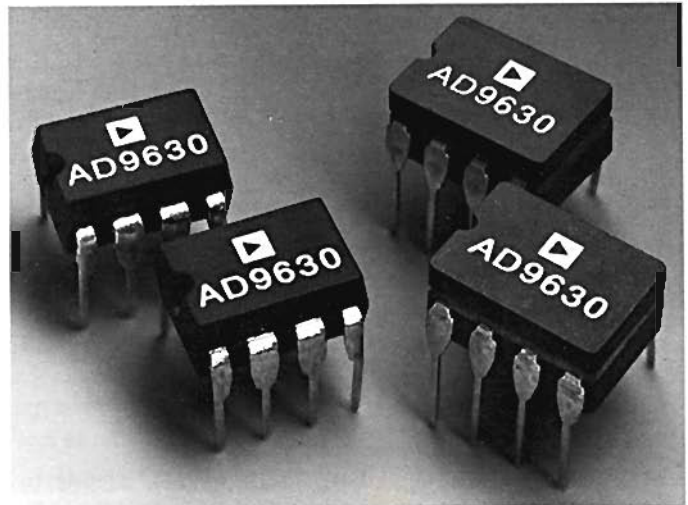


Figure 2. Large-signal pulse response.

\*Use the reply card for technical data.



-86, -75, and -46 dBc typical. Nonlinearity at dc and low frequencies is typically 0.03%.

Two grades of the AD9630 with identical specifications are available in a variety of 8-pin packages; the A and S grades differ only in operating temperature range, A:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  and S:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . All grades are available in Cerdip; the A grade is also available in plastic DIP and SOIC packages; and the S grade is available in a ceramic SOIC. Also available are devices in chip form and /883B versions of ceramic-packaged S-grade devices. The A version, in plastic DIP and SOIC, is priced at \$6.25 in 100s.

## APPLICATIONS

The AD9630 is an excellent choice to drive high-speed, high-resolution a/d converters. Its output stage is designed to drive high-speed flash converters using minimal (or no) series resistance. A current booster built into its output driver helps to maintain low distortion. Figure 3 shows the AD9630 driving the AD9060 10-bit, 75-MSPS flash converter. The 20-ohm series resistor is chosen to minimize frequency peaking.

The AD9630 was designed by Roy Gosser at Analog Devices' Computer Labs division, Greensboro, NC.

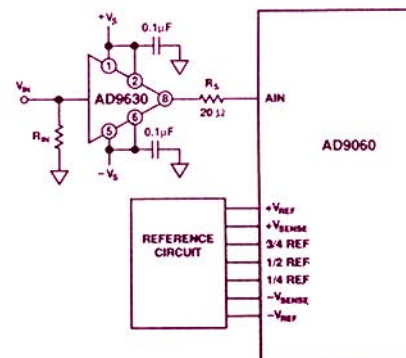


Figure 3. Driving the AD9060 a/d converter's signal input.

# CURRENT-OUTPUT MODULE AUGMENTS 6B SERIES

## 6B21 includes 12-bit DAC, RS-485 port, and microcontroller

### Has accuracy to within $\pm 0.02\%$ , nonlinearity $\pm 0.02\%$ of full-scale range

by Ian Bruce

The 6B21\* current-output module accepts RS-485 command signals from a host computer and converts serial data to a 0-to-20 mA or 4-to-20 mA digitally programmable output current, isolated from the digital input. Fully compatible with other 6B modules and backplanes and designed for industrial command-and-control applications, it can drive actuators, valves, recorders, and indicators, providing computations and communications, current-output readback and preset default conditions.

**6B Signal Conditioners:** The 6B family of configurable signal conditioners (*Analog Dialogue 23-1*) interfaces to a wide variety of analog and digital signals and sensors. The modules, employing high-density, low-cost surface-mount technology, are designed for a dedicated 1-, 4-, or 16-channel backplane—giving physical support, power, and a communications interface. 16 backplanes can be interconnected on a single multidrop link, for up to 256 channels of transducer I/O. 6B modules have converters, microcontrollers, non-volatile memory, and serial communications, and operate from a single +5-volt power supply. 6Bs include the 6B11 thermocouple/millivolt interface module, 6B12 analog interface, 6B13 resistance-temperature-detector (RTD) interface, and the 6B50 digital I/O board.

**Architecture:** The 6B21's RS-485 communications port is controlled by an 8052 microcontroller with non-volatile memory (EEPROM); the module also contains—fully isolated—a 12-bit DAC, a dc/dc converter for powering the current loop, and current-sensing and readback circuitry (Figure 1). The  $\mu\text{C}$  harbors the full command instruction set, controls the DAC, and performs many other functions. Isolated current-sensing circuitry allows recording of the actual load-loop current. *Readback* employs an opto-isolated voltage-to-frequency (V/F) converter; it measures the drop across a small current-measuring resistor and its frequency is directly proportional to the output current. Readback also detects open circuits in 4-to-20-mA applications.

**Performance:** The current output of the 6B21 can be scaled to 0-to-20 or 4-to-20 mA, with  $\pm 10\%$  overrange, into a load of 0 to 750  $\Omega$ . Factory-calibrated accuracy is to within  $\pm 0.02\%$  of full-scale reading (FSR), with a typical offset of only  $\pm 5 \mu\text{A}$ . Max nonlinearity is  $\pm 0.02\%$  FSR. Readback accuracy is to within  $\pm 0.5\%$  FSR, with a typical offset of  $\pm 100 \mu\text{A}$  and nonlinearity of 0.5% FSR. All connections have 1,500-V isolation, with 90-dB




common-mode rejection at 60 Hz and transient protection compliant with IEEE-STD 472 (SWC). The 6B21 can respond to 100 commands per second, and its settling time to 0.1% FSR is 5 ms. Quiescent current from the +5-volt supply is 250 mA.

**Calibration and Setup Commands:** The 6B21 has a wide range of commands for setup routines, system and circuit calibration, and fault-tolerant applications. All factory and user calibrations and settings are made through the serial port; so there is no need for any manual trims or adjustments. In addition to its absolute value, the *slew rate* of the current signal can be controlled at any value from 0.125 mA/s to 128 mA/s. A *setup* command programs the EEPROM to set the output to any predetermined level in case of power-cycling or brownout; *reset* is used to determine if the module has lost power; together they make the 6B21 particularly fault tolerant in systems using separate supplies for the host and signal-conditioners.

**Serial Communications:** The 6B21 communicates using an RS-485 bidirectional, half-duplex scheme with two wire-pairs—one for differential data; the other—a handshake line—for request-to-send (RTS), which controls the transmit/receive direction of in-line repeaters in multidrop schemes, extending the reach of a 6B system to over 4,000 feet for each inter-backplane segment.

The 6B21 plugs directly into the 6B backplane; it is encapsulated in a 2.3"  $\times$  3.1"  $\times$  0.75" module and fully specified over the industrial ( $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) temperature range. Its price is \$250.

The 6B21 was designed by Alan Jefferey at ADI's Industrial Products Division, Norwood, Mass. 

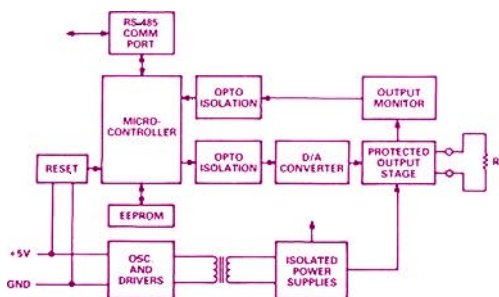


Figure 1. Functional block diagram of the 6B21.

\*Use the reply card for technical data.

# MONOLITHIC 12-BIT HIGH-SPEED A/D CONVERTER OPTIONS

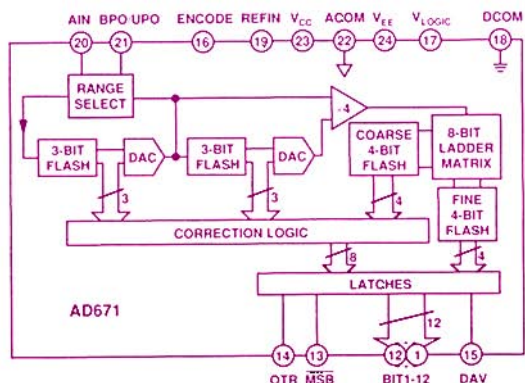
AD671 converts in choice of 500- or 750 ns max

AD7586 converts in 1  $\mu$ s with no missing codes over temperature

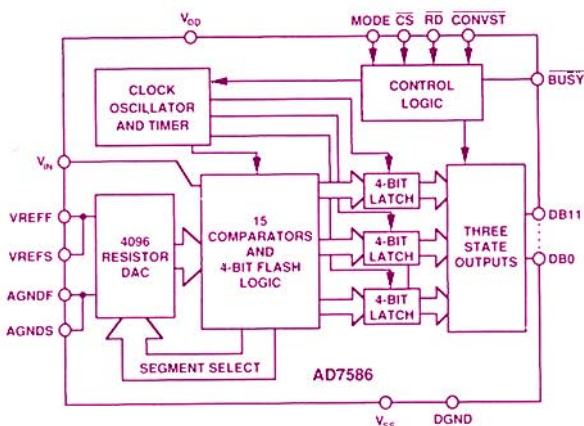
The AD671\* and AD7586\* families of monolithic analog-to-digital converters form a set of low-power, low-cost 12-bit ADCs that can fulfill most needs for sub- $\mu$ s conversions. Specification requirements for fast ADCs depend on the application, and the key spec is conversion speed; beyond this, cost, package size, and power dissipation are often important factors. So it's worth noting that these families are low in dissipation and cost and are of small size (especially the AD671, in the 0.3" "skinny DIP" package). Prices for both families start at \$65 in 100s (plastic).

The available choice of conversion speeds is defined in terms of maximum conversion time, ranging from 500 ns for the AD671-500 to 1  $\mu$ s for the AD7586. The table shows the principal trade-offs among the device grades introduced here:

	AD671JD-500	AD671JD-750	AD7586AQ	AD7586BQ
Conversion time	500 ns	750 $\mu$ s	1 $\mu$ s	1 $\mu$ s
No missing codes (bits)	10	11	12	12
Integral nonlinearity	$\pm 4$ LSB	$\pm 2$ LSB	$\pm 2$ LSB	$\pm 1.5$ LSB
Power dissipation, max	621 mW	621 mW	300 mW	300 mW
Package	24-pin 0.3" ceramic DIP		28-pin cardip	
Input signal range	$\pm 5$ V, 0 to +5 V, 0 to +10 V		0 to -4 V	
Price (100s)	\$75	\$75	\$75	\$90



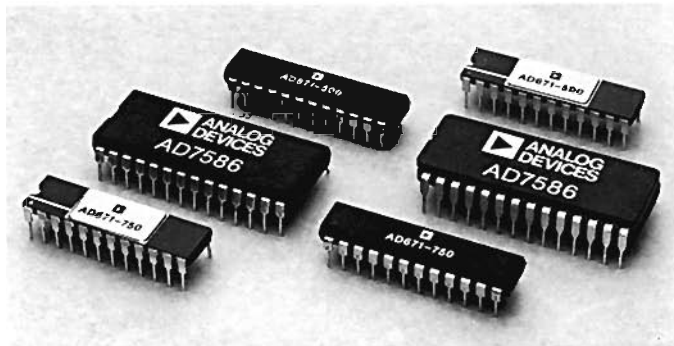
a. AD671 block diagram, showing four-step flash converters.



b. AD7586 block diagram, including monotonic segmented DAC and 3 four-bit flash converters. Note the force-sense reference connections.

Figure 1. Architectures of the AD671 and AD7586.

\*Use the reply card for technical data.



Typical applications for this level of performance include charge-coupled devices (CCDs), photomultipliers, infrared (IR) detectors, and multi-channel analog I/O. Communication systems can benefit, for example, high-speed modems, baseband signal analysis, and cellular phone base systems. And there are many more, including high-speed data acquisition for PCs, waveform analyzers, image scanners, medical instruments, etc.

**AD671** is the fastest commercially available monolithic 12-bit a/d converter. It is used in systems where compromises are not possible in conversion speed, choice of input signal range, power dissipation, and board space. It replaces hybrid converters and discrete digitizing circuits in high-speed data-acquisition circuits.

Besides its basic performance, achieved by a 4-cycle flash sub-ranging technique with digital error correction (Figure 1a), a few unique features enhance its usefulness. The input circuit allows choice among standard instrumentation-level ranges and is designed for a standard +5-volt reference. The output for bipolar inputs is offset binary and twos complement—no need for the time-skewed delay of an extra inverting gate. An out-of-range output indicates saturation—this facilitates range-switching in programmable-gain front ends.

In sampling systems, when used with a discrete sample/hold amplifier built into its evaluation board, and sampled at 1 MHz, the AD671 typically has -80 dB of total harmonic distortion for signals from dc to 100 kHz, with  $S/(N+D)$  of 70 dB—and distortion of -75 dB for 500 kHz, with  $S/(N+D)$  of 68 dB.

The **AD7586**, a high-performance general-purpose 12-bit converter, fits into any application calling for processing of high-frequency signals or rapid multiplexing of many channels. Fabricated in LC<sup>2</sup>MOS, it performs full 12-bit conversions in 1  $\mu$ s and consumes only 300 mW with no missing codes over the temperature range and only 1.5 LSB of linearity error (B version). Its 57-ns data-access time allows it to interface directly with all standard digital signal processors (DSPs).

The AD7586's reference terminals (Figure 1b) have Kelvin "force-sense" connections, minimizing offset and gain errors. Using an external sample/hold, and sampling a 100-kHz sine wave at 300 kps, SNR is 70 dB, with total harmonic distortion of -81 dB.

The AD671 was designed by Doug Mercer and Mike Timko at Analog Devices Semiconductor, Wilmington MA; the AD7586 was designed by Mike Tuhill at Analog Devices BV, Limerick, Ireland. ▶



# INDUSTRIAL PROCESS CONTROLLER IS PROGRAMMABLE IN C

$\mu$ MAC-1060 integrates CPU, ADC, analog/digital I/O in one package

Unit functions autonomously for embedded applications

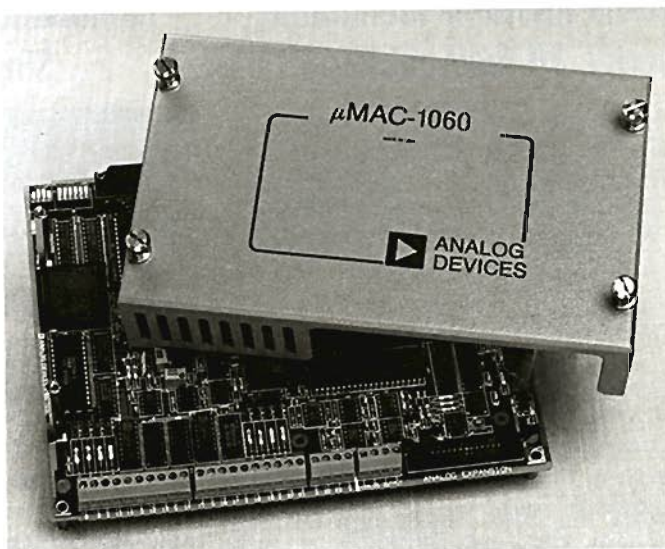
The  $\mu$ MAC-1060\* is an input/output (I/O) controller for industrial processes that require both monitoring and control. A single-board device, it handles analog I/O (sensors, actuators), digital I/O (on/off), and pulse I/O (event counting, time-proportional output); in system applications, its capacity can be easily expanded to additional channels beyond the capacity of the basic board.

Although the  $\mu$ MAC-1060 is very similar to the  $\mu$ MAC-1050 in hardware (*Analog Dialogue* 23-4), the user software is significantly different. The key distinction is that the  $\mu$ MAC-1060 is programmed by the user in the C language (using the integral measurement and control commands), to produce a compact final application program. This allows sophisticated users and system integrators to take maximum advantage of the  $\mu$ MAC-1060's potential and add unique value to the final delivered package.

The user-developed  $\mu$ MAC-1060 program is resident on-board, stored either in battery-backed RAM or burned into EPROM. As a result, the  $\mu$ MAC-1060 can be used autonomously as a dedicated, *embedded* controller, without any user terminal or workstation. Nevertheless, it can connect to a user interface or network (up to 64  $\mu$ MAC-1060s on a single link, if desired), via RS-232, -422, or -485 standards. In contrast, the  $\mu$ MAC-1050 requires a host and cannot function independently.

**Analog/Digital Conversion:** The base unit provides eight differential or 16 single-ended analog inputs, with accommodations for a variety of isolated or non-isolated I/O expansion options (for thermocouples, strain gages, high- and low-level voltages, current loop signals). Up to 80 inputs can ultimately be handled. All analog inputs are converted with an integrating 18-bit a/d converter.

Integration periods and resolutions, individually selectable for each channel, range from 550  $\mu$ s/13bits (effective throughput of 359 samples per second) to 20 ms/18 bits (44 sps), allowing the user to maximize throughput while maintaining desired resolution. The system also monitors an internal reference voltage and analog ground, automatically calibrating itself to eliminate the effects of drift in the input section.



A built-in SBX (Small Bus eXpansion) port is available for additional serial communications and for applications with unique requirements not directly served by the  $\mu$ MAC-1060. This user-programmable port accommodates standard single- or double-width SBX boards, for applications such as networking or data-logging; an optional SBX board with two serial ports is available.

**Program Development:** Applications programs are developed using an IBM PC/XT/AT or PS/2, or equivalent, with Aztec C86 Commercial System from Manx as the C compiler. A Terminal Emulator and Downloader module allows the PC to be used as a terminal to configure the  $\mu$ MAC-1060 communications, select directories, select files to download, and log serial-port inputs.

The programmer can also invoke a Debugger for breakpoint setting and single-step execution, as well as display of memory and disassembled code. Immediate-mode control-function commands can be invoked aside from an executing application program, useful for setup, debugging, and verifying cause/effect.

**Run-Time Communications:** Although the  $\mu$ MAC-1060 is intended to run autonomously, connection to a host computer as higher-level supervisor is often necessary. The  $\mu$ MAC-1060 supports several run-time communications protocols, including an efficient binary protocol—which transfers run-time data with high effective throughput rates. For supervisory programs in Microsoft or Turbo C, measurement and control communications software (MACCS) is available with this protocol. In addition,  $\mu$ MAC-1050s and  $\mu$ MAC-1060s can coexist on a serial link and communicate via a C-based application program.

The  $\mu$ MAC-1060 is housed on a single 7"  $\times$  9" circuit board and requires a +5-V power supply; all field wiring is attached via screw terminals. The price is \$1,295 for a 32K version, \$1,395 for 128K.

The  $\mu$ MAC-1060 hardware was designed by Tom Kelly and the software was integrated by Raouf Bortosh. Both are with Analog Devices' Industrial Products Division, Norwood, Massachusetts.  $\blacksquare$

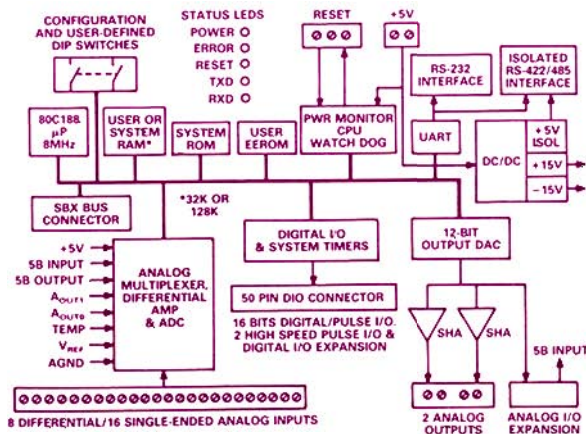
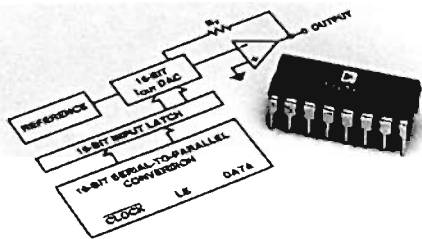


Figure 1. Block diagram of the  $\mu$ MAC-1060.

\*Use the reply card for technical data.

## DIRECT DSP DAC

16-bit AD766 is monolithic  
Serial, 16-lead package



The AD766\* is a complete, monolithic 16-bit digital-to-analog converter specifically designed for direct, "no-glue-logic" interfacing to the serial ports of digital signal processors, such as the ADSP-2101, TMS320 series, and DSP56000, at word rates up to 500 kbps.

Typical applications include signal processing for computers and peripherals, high-end modems, sonar signal processing, noise cancellation, speech synthesis, and many others.

Three lines form the complete interface: clock, data, and latch enable. The 16-bit twos-complement word arrives, MSB first; and the data bits are clocked into the input register on the falling edge of the clock signal, at bit rates up to 12.5 MHz. Once the LSB has been clocked in, a *latch enable* pulse updates the DAC input, which is converted to a high-quality analog voltage, settling to 0.0015% FSR in 1.5  $\mu$ s. Current settling is even faster, 350 ns.

The AD766 is a *complete* DAC, comprising the basic 16-bit DAC, a reference, output amplifier, and serial-to-parallel input register. It uses  $\pm 5$ - to  $\pm 12$ -volt supplies, and its signal output range is  $\pm 3$  V.

Over the full temperature range, signal-to-noise ratio is 94 dB min, 20 Hz to 20 kHz, and 79 dB min for frequencies up to 250 kHz. THD at 1,037 Hz is -81 dB for a 0-dB signal. No-missing-codes resolution is 15 bits.

With only 120 mW of dissipation, the AD766JN, for 0 to +70°C, is available in a 16-pin plastic DIP. Other temperature ranges and packages, including /883, are planned. Prices (100s) start at \$11. ▶

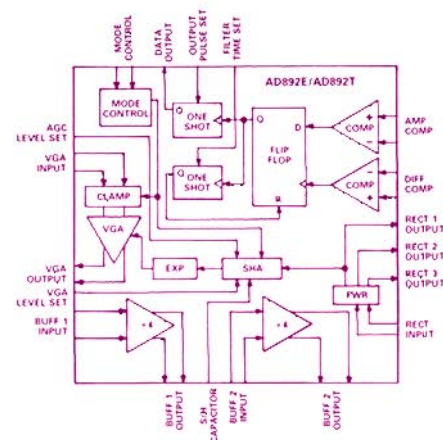
\*Use the reply card for technical data.

## 30 Mb/s PEAK DETECTOR FOR DISK DRIVES

Monolithic AD892 versions are available for TTL and ECL  
Single-chip solution for 3.5" and 5.25" disk drives

The AD892\* is a complete monolithic subsystem for recovering binary information from differentiating channels (such as disk-drive pickup heads) with transfer rates of up to 30 megabits per second. It receives corrupted binary signals from the read-head amplifier and performs signal conditioning and data qualification to produce recovered bits ready for synchronization.

It has a variable-gain amplifier (VGA), gain-of-four precision buffers, sample/hold (S/H) circuitry, automatic gain control, dynamic clamp, laser-trimmed comparators, and precision one-shots for low pulse pairing and consequently low bit-error-rate (BER) performance (<1-ns additional pulse pairing guaranteed) in the electronically difficult disk environment. In effect, it combines on a single chip the functions of the (50-megabit) AD890 and AD891, introduced in *Analog Dialogue* 22-1, 1988, pp. 3-6.



Two versions are available: the 30-Mb/s AD892E (differential ECL data output) and the TTL-compatible 25-Mb/s AD892T. Operation is from +5- and +12-volt supplies. The device is packaged in a 44-pin PLCC. Price in OEM quantities is <\$5.00. ▶

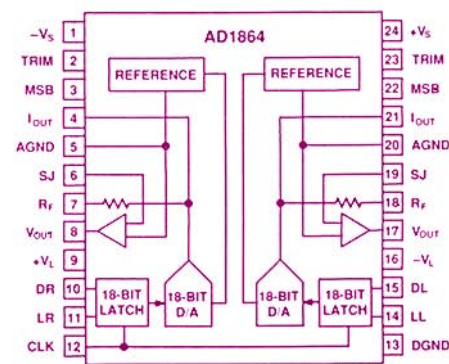
## MONOLITHIC DUAL 18-BIT AUDIO DAC

AD1864 is complete — no external components  
100% tested at 8 $\times$  oversampling per channel

The AD1864\* is a complete (no external components) monolithic dual-channel 18-bit voltage-output d/a converter for audio applications. It includes two independent serial-input 18-bit DACs with references, latches, and output amplifiers (with feedback resistors), and a common clock line.

An 18-bit dual-channel DAC provides high performance with reduced cost, space, and power requirements in such multichannel audio applications as compact-disc players, multi-voice keyboard instruments, digital-audio tape recorders and players, digital mixing consoles, and multimedia workstations. The AD1864's  $\pm 5$  to  $\pm 12$ -volt power-supply range (dissipating only 225 mW) adds a dimension of flexibility.

Performance is the reason for using 18-bit DACs, and the AD1864 fulfills the expectation, providing co-phased outputs with: 115 dB (110 min) of channel separation; 2% max gain error with 0.3% channel-to-channel gain matching; 0.006% total har-



monic distortion & noise (THD+N) at 0 dB. Other specs include min SNR of 102 dB and typical midscale error of 4 mV, with 5-mV matching. All devices are tested at 8 $\times$  oversampling per channel, where 44.1 kHz is the basic sampling frequency.

In the 28-pin plastic DIP package, three performance grades are available for 0 to 70°C operation, the AD1864N, N-J, and N-K, with max THD+N of 0.006%, 0.004%, and 0.0025%. Prices (1,000) start at \$14.25. ▶

## DATA-ACQUISITION I/O BOARD FOR PC/XT/AT

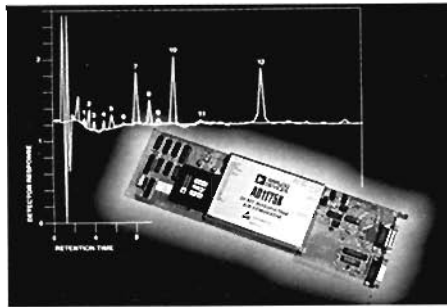
RTI-870 has 22 bits of resolution, samples at 20 Hz

Up to four analog inputs can be multiplexed

The RTI-870\* is a high-resolution data-acquisition plug-in board for the IBM PC/XT/AT designed especially for chromatography applications. With its dedicated software, the RTI-870 can transform the computer into a fully functioning chromatography workstation that can use any popular DOS analysis or graphics software program.

It provides 22-bit resolution, with 0.5-ppm nonlinearity,  $<2 \mu\text{V}$  of noise, and 0.005% gain error, for sampling at up to 20/s (in 60-Hz systems, 15/s for 50 Hz). Needing only a single slot in the PC backplane, the RTI-870 can record data from four sources. Software-programmable gain allows input scaling ranges of  $\pm 100 \text{ mV}$ ,  $\pm 1$  and  $\pm 5 \text{ V}$ , selectable each time a reading is taken.

The board comes complete with LABTECH ACQUIRE®, a menu-driven data-acquisition software package. All raw data is sampled, converted, and automatically stored on disk or in PC memory. Optional



packages, such as LABTECH CHROM, can be used to smooth data, detect peaks, calculate peak height and area, and perform deconvolution and comparison-matching. Further analysis and report generation can be done with any popular DOS program capable of reading ASCII or DIF files.

Eight digital I/O lines are provided for control. An optional terminator, STB-CHR can be used for screw-terminal connections. Price of the RTI-870 (1s) is \$1,795. LABTECH CHROM adds \$495, and the STB-CHR is \$295. ▶

## HIGH SPEED MONOLITHIC DUAL OP AMP

AD827 combines two AD847s on a single chip

50-MHz bandwidth, 300-V/ $\mu\text{s}$  slew rate

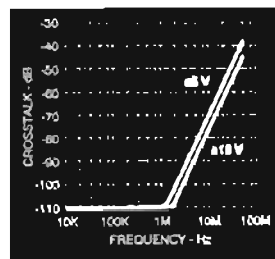
The AD827\* incorporates a pair of AD847 high-speed op amps in 8-pin DIP and 16-pin surface-mount packages. The devices are fully specified for operation using  $\pm 5$  to  $\pm 15$ -volt supplies.

They are useful wherever multiple wide-band op amps are needed. Of especial interest are applications calling for good differential phase and gain, as well as reasonable dc performance—applications such as video, special effects, color copiers, and ECM, radars, and heads-up displays.

Salient performance characteristics include:

- 50-MHz unity-gain bandwidth (stable at  $G=1$ ), necessary in video buffers
- 300-V/ $\mu\text{s}$  slew rate and 120-ns settling time, necessary in ADC and DAC buffering and pulse-handling applications
- 0.04% differential gain and  $0.19^\circ$  differen-

\*Use the reply card for technical data.



tial phase errors, important specs for video applications (see pages 12-13)

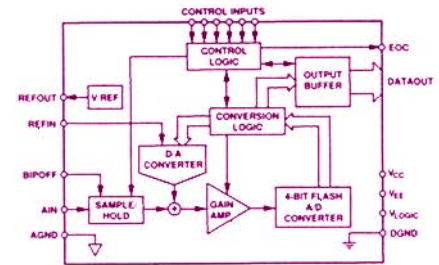
- dc specs: 2 mV max  $V_{os}$  and  $15 \mu\text{V}/^\circ\text{C}$  drift
- can drive unlimited capacitive loads stably
- low-supply-voltage operation.

The AD827 is available in J/A/S grades for the commercial, extended industrial, and military temperature ranges. The A and S grades are packaged in 8-pin cerdip, and the J grades are available in 8-pin plastic DIPs and 16-pin plastic small-outline packages. Prices start at \$4.50 in 1,000s. ▶

## SAMPLING ADC

200 KSPS, 12 bits

AD678: AC & DC specs



The AD678\* is a 12-bit, 200-kSPS sampling analog-to-digital conversion system, complete on a single bipolar-CMOS (BiMOS) chip. It includes an a/d converter, sample/hold, reference, clock, logic, and output buffer. Its input span is 10 volts, and it has a high ( $10\text{-M}\Omega$ ) input impedance.

Unlike most 12-bit ADCs, which are characterized in terms of either "dc" specs (offset, gain error, nonlinearity) or "ac" specs (signal-to-noise and distortion)—the AD678 K, B, & T are characterized *both* ways. This universal set of specs makes the AD678 useful in both signal processing and measurement/control/data acquisition—in short, wherever an application calls for a 12-bit ADC plus a sample/hold. It directly replaces the AD1678: with improved specs and a lower price.

Here are some examples of the AD678K's specs over temperature (0 to  $+70^\circ\text{C}$ ):

- AC: total harmonic distortion  $-80 \text{ dB}$  max; peak spurs  $-80 \text{ dB}$  max; signal to (noise + distortion)  $72 \text{ dB}$  min; full linear signal bandwidth  $500 \text{ kHz}$  min.
- DC: integral nonlinearity  $\pm 1 \text{ LSB}$  max; no missing codes; bipolar zero error  $\pm 3 \text{ LSB}$  max; gain error  $\pm 6 \text{ LSB}$  max, reference included. Zero and gain drift: 4, 6 LSB max.

The AD678 can interface directly to a 16-bit data bus, or to an 8-bit bus in an 8+4 format—right- or left justified. It uses  $\pm 12$ -volt ( $\pm 5\%$ ) and  $+5$ -volt ( $\pm 10\%$ ) supplies, with max power consumption of  $745 \text{ mW}$ .

The AD678 is currently available in J,K grades for 0 to  $70^\circ\text{C}$ ; A,B grades, for  $-40$  to  $+85^\circ$ , and S,T grades ( $-55$  to  $+125^\circ\text{C}$ ) will be available soon. J,K grades are packaged in 28-lead ceramic and plastic DIPs. Prices for AD678JN/KN are \$27/\$33 in 100s. ▶

# Ask the Applications Engineer—7

by James Bryant and Lew Counts

## OP-AMP ISSUES—NOISE

*Q. What should I know about op-amp noise?*

A. First, we must note the distinction between noise generated in the op amp and its circuit components and *interference*, or unwanted signals and noise arriving as voltage or current at any of the amplifier's terminals or induced in its associated circuitry.

Interference can appear as spikes, steps, sine waves, or random noise, and it can come from *anywhere*: machinery, nearby power lines, r-f transmitters and receivers, computers, or even circuitry within the same equipment (for example, digital circuits or switching-type power supplies). Understanding it, preventing its appearance in your circuit's neighborhood, finding how it got in, and rooting it out, or finding a way to live with it is a big subject. It's been treated in these pages in the past; those, and a few additional references, are mentioned in the Bibliography.

If all interference could be eliminated, there would still be random noise associated with the operational amplifier and its resistive circuits. It constitutes the ultimate limitation on the amplifier's resolution. That's the topic we'll begin to discuss here.

*Q. O.K. Tell me about random noise in op amps. Where does it come from?*

A. Noise appearing at the amplifier's output is usually measured as a voltage. But it is generated by both voltage- and current sources. All internal sources are generally referred to the input, i.e., treated as uncorrelated—or *independent*—random noise generators (see next question) in series or parallel with the inputs of an ideal noise-free amplifier: We consider 3 primary contributors to noise:

- a noise *voltage* generator (like offset voltage, usually shown in series with the noninverting input)
- two noise-*current* generators pumping currents out through the two differential-input terminals (like bias current).
- If there are any resistors in the op-amp circuit, they too generate noise; it can be considered as coming from either current sources or voltage sources (whichever is more convenient to deal with in a given circuit).

Op-amp voltage noise may be as low as  $3 \text{ nV}/\sqrt{\text{Hz}}$ . Voltage noise is the noise specification that is more usually emphasized, but, if impedance levels are high, current noise is often the limiting factor in system noise performance. That is analogous to offsets, where offset voltage often bears the blame for output offset, but bias current is the actual guilty party. Bipolar op-amps have traditionally had less *voltage* noise than FET ones, but have paid for this advantage with substantially greater *current* noise—today, FET op-amps, while retaining their low current noise, can approach bipolar voltage-noise performance.

*Q. Hold it!  $3 \text{ nV}/\sqrt{\text{Hz}}$ ? Where does  $\sqrt{\text{Hz}}$  come from? What does it mean?*

A. Let's talk about random noise. Many noise sources are, for practical purposes (i.e., within the bandwidths with which the designer is concerned), both white and Gaussian. White noise is noise whose power within a given bandwidth is independent of frequency. Gaussian noise is noise where the probability of a particular amplitude,  $X$ , follows a Gaussian distribution. Gaussian

noise has the property that when the rms values of noise from two or more such sources are added, provided that the noise sources are uncorrelated (i.e., one noise signal cannot be transformed into the other), the resulting noise is not their arithmetic sum but the root of the sum-of-their-squares (RSS).\* The RSS sum of three noise sources,  $V_1$ ,  $V_2$ , and  $V_3$ , is

$$V_0 = \sqrt{V_1^2 + V_2^2 + V_3^2}$$

Since the different frequency components of a noise signal are uncorrelated, a consequence of RSS summation is that if the white noise in a brick-wall bandwidth of  $\Delta f$  is  $V$ , then the noise in a bandwidth of  $2 \Delta f$  is  $\sqrt{V^2 + V^2} = \sqrt{2} V$ . More generally, if we multiply the bandwidth by a factor  $K$ , then we multiply the noise by a factor  $\sqrt{K}$ . The function defining the rms value of noise in a  $\Delta f = 1 \text{ Hz}$  bandwidth anywhere in the frequency range is called the (voltage or current) *spectral density function*, specified in  $\text{nV}/\sqrt{\text{Hz}}$  or  $\text{pA}/\sqrt{\text{Hz}}$ . For white noise, the spectral density is constant; it is multiplied by the square root of the bandwidth to obtain the total rms noise.

A useful consequence of RSS summation is that if two noise sources are contributing to the noise of a system, and one is more than 3 or 4 times the other, the smaller is often ignored, since

$$\sqrt{4^2} = \sqrt{16} = 4, \text{ while } \sqrt{4^2 + 1^2} = \sqrt{17} = 4.12$$

[difference less than 3%, or 0.26 dB]

$$\sqrt{3^2} = \sqrt{9} = 3, \text{ while } \sqrt{3^2 + 1^2} = \sqrt{10} = 3.16$$

[difference less than 6%, or 0.5 dB]

The source of the higher noise has become the *dominant* source.

*Q. O.K. How about current noise?*

A. The current noise of simple (i.e. not bias-current-compensated) bipolar and JFET op-amps is usually within 1 or 2 dB of the Schottky noise (sometimes called the "shot noise") of the bias current; it is not always specified on data sheets. Schottky noise is current noise due to random distribution of charge carriers in the current flow through a junction. The Schottky noise current,  $I_n$ , in a bandwidth,  $B$ , when a current,  $I$ , is flowing is obtained from the formula

$$I_n = \sqrt{2IqB}$$

Where  $q$  is the electron charge ( $1.6 \times 10^{-19} \text{ C}$ ). Note that  $\sqrt{2Iq}$  is the spectral density, and that the noise is white.

This tells us that the current noise spectral density of simple bipolar transistor op-amps will be of the order of  $250 \text{ fA}/\sqrt{\text{Hz}}$ , for  $I_b = 200 \text{ nA}$ , and does not vary much with temperature—and that the current noise of JFET input op-amps, while lower ( $4 \text{ fA}/\sqrt{\text{Hz}}$  at  $I_b = 50 \text{ pA}$ ), will double for every  $20^\circ\text{C}$  chip temperature increase, since JFET op-amps' bias currents double for every  $10^\circ\text{C}$  increase.

Bias-compensated op-amps have much higher current noise than one can predict from their input currents. The reason is that their net bias current is the *difference* between the base current of the input transistor and the compensating current source, while the noise current is derived from the RSS *sum* of the noise currents.

[\*Note the implication that noise *power* adds linearly (sum of squares).]

Traditional voltage-feedback op-amps with balanced inputs almost always have equal (though uncorrelated) current noise on both their inverting and non-inverting inputs. Current-feedback, or transimpedance, op-amps, which have different input structures at these two inputs, do not. Their data sheets must be consulted for details of the noise on the two inputs.

The noise of op-amps is Gaussian with constant spectral density, or "white", over a wide range of frequencies, but as frequency decreases the spectral density starts to rise at 3 dB/octave. This low-frequency noise characteristic is known as "1/f noise" since the noise *power* spectral density goes inversely with frequency. It has a -1 slope on a log plot (the noise *voltage* (or *current*)  $1/\sqrt{f}$  spectral density slopes at -1/2). The frequency at which an extrapolated -3 dB/octave spectral density line intersects the mid-frequency constant spectral density value is known as the "1/f corner frequency" and is a figure of merit for the amplifier. Early monolithic IC op-amps had 1/f corners at over 500 Hz, but today values of 20-50 Hz are usual, and the best amplifiers (such as the AD-OP27 and the AD-OP37) have corner frequencies as low as 2.7 Hz. 1/f noise has equal increments for frequency intervals having equal ratios, i.e., per *octave* or per *decade*.

*Q: Why don't you publish a noise figure?*

*A:* The noise figure (NF) of an amplifier (expressed in dB) is a measure of the ratio of the amplifier noise to the thermal noise of the source resistance.

$$V_n = 20 \log \{ [V_n(\text{amp}) + V_n(\text{source})] / V_n(\text{source}) \}$$

It is a useful concept for r-f amplifiers, which are almost always used with the same source resistance driving them (usually 50  $\Omega$  or 75  $\Omega$ ), but it would be misleading when applied to op amps, since they are used in many different applications with widely varying source impedances (which may or may not be resistive).

*Q: What difference does the source impedance make?*

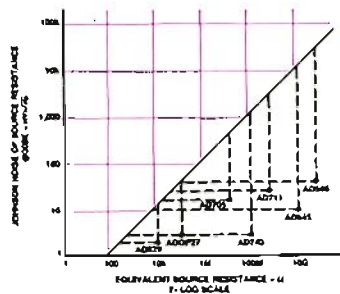
*A:* At temperatures above absolute zero all resistances are noise sources; their noise increases with resistance, temperature, and bandwidth (we'll discuss basic resistance noise, or *Johnson noise*, in a moment). *Reactances* don't generate noise, but noise currents through them will develop noise voltages.

If we drive an op-amp from a source resistance, the equivalent noise input will be the RSS sum of the amplifier's noise voltage, the voltage generated by the source resistance, and the voltage caused by the amplifier's  $I_n$  flowing through the source impedance. For very low source resistance, the noise generated by the source resistance and amplifier current noise would contribute insignificantly to the total. In this case, the noise at the input will effectively be just the voltage noise of the op-amp.

If the source resistance is higher, the Johnson noise of the source resistance may dominate both the op-amp voltage noise and the voltage due to the current noise; but it's worth noting that, since the Johnson noise only increases with the square root of the resistance, while the noise voltage due to the current noise is directly proportional to the input impedance, the amplifier's current noise will always dominate for a high enough value of input impedance. When an amplifier's voltage and current noise are high enough, there may be no value of input resistance for which Johnson noise dominates.

This is demonstrated by the figure below, which compares voltage and current noise for several Analog Devices op amp types,

for a range of source-resistance values. The diagonal line plots vertically the Johnson noise associated with resistances on the horizontal scale. Let's read the chart for the ADOP27: The horizontal line indicates the ADOP27's voltage noise level of about 3 nV/ $\sqrt{\text{Hz}}$  is equivalent to a source resistance of less than about 500  $\Omega$ . Noise will not be reduced by (say) a 100- $\Omega$  source impedance, but it will be increased by a 2-k $\Omega$  source impedance. The vertical line for the ADOP27 indicates that, for source resistances above about 100 k $\Omega$ , the noise voltage produced by amplifier's current noise will exceed that contributed by the source resistance; it has become the dominant source.



Remember that any resistance in the non-inverting input will have Johnson noise and will also convert current noise to a noise voltage; and Johnson noise in feedback resistors can be significant in high-resistance circuits. All potential noise sources must be considered when evaluating op amp performance.

*Q. You were going to tell me about Johnson noise.*

*A.* At temperatures above absolute zero, all resistances have noise due to thermal movement of charge carriers. This is called Johnson noise. The phenomenon is sometimes used to measure cryogenic temperatures. The voltage and current noise in a resistance of  $R$  ohms, for a bandwidth of  $B$  Hz, at a temperature of  $T$  kelvins, are given by:

$$V_n = \sqrt{4kTRB} \text{ and } I_n = \sqrt{4kTB/R}$$

Where  $k$  is Boltzmann's Constant ( $1.38 \times 10^{-23}$  J/K). A handy rule of thumb is that a 1-k $\Omega$  resistor has noise of 4 nV/ $\sqrt{\text{Hz}}$  at room temperature.

All resistors in a circuit generate noise, and its effect must always be considered. In practice, only resistors in the input(s) and, perhaps, feedback, of high-gain, front-end circuitry are likely to have an appreciable effect on total circuit noise.

Noise can be reduced by reducing resistance or bandwidth, but temperature reduction is generally not very helpful unless a resistor can be made very cold—since noise power is proportional to the *absolute* temperature,  $T = ^\circ\text{C} + 273^\circ$ . ■

(to be continued)


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# Worth Reading

## BOOK REVIEWS

Prentice Hall has just published *Digital Signal-Processing Applications Using the ADSP-2100 Family* in hardcover. Written by the Applications Staff of Analog Devices' DSP Division and edited by Amy Mar, it is about bridging the gap between DSP algorithms and implementing them on state-of-the-art digital signal processors. Each chapter tackles a specific application topic, describing the algorithm and discussing its implementation with the ADSP-2100 family. Comprehensive source-code listings are included, with comments and explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. It is available from Analog Devices (the \$38 price includes two floppy disks)—use the book mailing card; or with VISA, call (617) 329-4700, ext. 3392.

Application topics include the basics of multiprecision math on a 16-bit device, fixed-coefficient and adaptive filtering, FFT implementation, image processing, graphics, linear predictive speech encoding (LPC), pulse-code modulation (PCM) and adaptive differential PCM, dual-tone multifrequency (DTMF), and sonar beamforming. Also included: the basic architecture of the ADSP-2100 processor family and hardware issues when interfacing with memory, other processors, and host computers. The book is an ideal companion to *Digital Signal Processing in VLSI*, by Richard J. Higgins, also available from ADI. 

ADI's *High-Speed Design Seminar* notes (1990), 500 pages of solid, practical information, are now available for \$20—use the book mailing card; for VISA, call (617) 329-4700, ext. 3392. 

## FREE CATALOGS & MANUALS\*

**ADSP-2101/2102 User's Manual:** new edition available.

**1990 Data Acquisition and Control Catalog.** 258 pages with complete product descriptions, configuration charts, block diagrams, specifications, and pricing for sensor-to-host subsystems. Included: modular signal conditioners, PC-compatible data-acquisition adapter boards, distributed data-acquisition-and-control hardware, and applications software.

**1990 Military Products Databook:** 1,076 pages of useful information on more than 200 amplifier, data-converter, analog- and digital signal processing product families, with JAN and SMD cross-references and much additional data.

## FREE SERIAL PUBLICATIONS\*

**DSPatch—The DSP Applications Newsletter:** No. 15, spring 1990 (32 pp.), introduces the ADSP-21msp50 mixed-signal processor, the low-cost ADSP-2105, and the HIP-equipped ADSP-2111—all introduced at IEEE ICASSP 90. Also: use of the ADSP-2100 family in the Nikon Full Color Printer and the Androx ICS-400 image computer; new tools for the ADSP-2101: ADSP-2101 Emulator, low-cost EZ-ICE™ in-circuit emulator, EZ-LAB™ evaluation and demo board; articles on V.32 modem algorithms (ADSP-2101 implementation); development process for ADSP-2100 family applications, more on sigma-delta conversion; and GSM Digital Mobile Radio.

**A Special Issue** (28 pp.) collects reprints of *DSPatch* stories describing customer uses of Analog Devices DSP products.

\*Available free upon request.

**Analog Briefings—The Newsletter for Military/Avionics Industry,** 6-1, spring 1990, discusses relevant Notice 8 changes to MIL-STD-883 and Amendment 3 of MIL-M-38510 relating to ESDS classification. Describes new products, including: the AD203 rugged standalone (*no dc-dc converter necessary*) isolation amplifier for the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range; the ADSP-1010B 16x16-bit multiplier/accumulator and its Standard Military Drawing (SMD) 5962-88733; the 6S04 Digital Director Unit, for synchro-based servo testing; and /883 qualification for AD2S80 monolithic resolver-to-digital converter.

## APPLICATION NOTES\*

**"A function generator and linearization circuit using the AD7569,"** by James Bryant. Using the AD7569 monolithic 8-bit analog I/O port (*Analog Dialogue* 21-2, pp. 3-5) and an EEPROM to generate arbitrary nonlinear *analog-to-analog* functions.

**"Understanding and applying the AD7341/AD7371 switched-capacitor filters,"** by John Reidy & Mike Curtin. Useful information on these devices (*Analog Dialogue* 23-2, pp. 7-10).

## MORE AUTHORS (Continued from page 2)

**Scott Wurcer** (page 12), a Senior Design Engineer at Analog Devices Semiconductor, has been with the company for 15 years. Responsible for designing op amps and other linear ICs, he has designed the AD711 family and the AD744 op amps, and the AD524 and AD624 instrumentation amplifiers. Scott has a BSEE from MIT and is a member of IEEE and AES. In his spare time, he enjoys carpentry and non-commercial music.




**Jeff Smith** (page 12) is a Senior Design Technician in the Amplifier Design Group at ADS, Wilmington, MA. He received a Bachelor of Arts in Music Theory and Composition from Brandeis University—and expects to complete a BSEE from Northeastern University before the millennium. He enjoys alternate music styles and preparing and cooking sausage.



**Ian Bruce** (page 15) is a Senior Technical Marketing Engineer in the Marketing Communications Group in Norwood, MA. In over 5 years with Analog Devices, he has worked in design, marketing, and sales in the USA and England (his native country). Ian holds a BSc degree in Electrical Engineering from Coventry College. His interests include reading, travel, and a reluctant old MG sports car.



**Cover design:** The front-cover pictorial of this issue of *Analog Dialogue* symbolizes an application of the ADSP-21msp50 Mixed-Signal Processor in digital mobile telephony. It was designed and executed by Shelley Cohane, of Design Encounters, Hingham, Massachusetts. 

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

## STOP PRESS—NEWLY ANNOUNCED PRODUCTS: . . .

The ADV7121\*—in a 40-pin plastic DIP—and ADV7122\*—in a 44-pin PLCC—are Monolithic Triple 10-Bit DACs for video applications with grades for clock rates up to 30, 50, and 80 MHz. The ADV7120,\* for applications with the same clock rates but less demanding resolution, is a Monolithic Triple-8-Bit Video DAC . . . The ADSP-2105\* is a low-cost pin- and code-compatible version of the ADSP-2101 DSP,\* with a single serial port and one-half the on-chip memory . . . The ADSP-2111\* is a code-compatible version of the ADSP-2101 DSP with the addition of a host interface port (see page 4, this issue) . . . EZ-ICE™\*, EZ-LAB™\*, and EZ-KIT™\* are low-cost, easy-to-use development tools for the ADSP-2101 and ADSP-2105 microcomputers. EZ-ICE is an In-Circuit Emulator and EZ-LAB is a Demonstration and Evaluation Board, and EZ-KIT is an EZ-LAB board with cross-software . . . The AD645\* is a low-cost, low-noise (9 nV/√Hz, 0.6 fA/√Hz), low-bias-current (1.5 pA max) Op Amp . . . The AD694\* converts a single-ended high-level analog input voltage to the 4-to-20-mA current transmission format accurately and at low cost . . . The DMB-PULSE I/O Panel for industrial process controllers expands event counters, frequency inputs, time-proportional outputs.

## PRODUCT NOTES . . . AD586 and AD587 Voltage References

are now available in plastic 8-pin mini-DIP packages. CWYLSO† . . . Now converted to cerdip (Q) packaging instead of side-brazed (D): AD7520T/U (and S/T/U /883 versions), AD7521J (and S/T/U /883 versions), AD7522S (and S/T /883 versions), AD7525B (and B /+ version), AD7543B (and B /+ version), AD7543T (and T & GT /883 versions), and AD7549A/B/S/T (and S/T /883 versions). CWYLSO† . . . There is a new revision of the 6B Series Ordering Guide (B1243a-10-3/90)\* . . . For a 6B Series demo disk, CWYLSO† . . . The 6B Series Configuration Disk has been upgraded to Rev 2.02, supporting 6B13, 6B21, and 6B50; it includes Turbo Pascal 5.0 and 5.5 driver modules. Driver upgrades for THE FIX and Control EG to support these are now available; and we expect LABTECH upgrades to be available soon. CWYLSO† . . . Model 171J/K FET-Input High-Voltage Op Amp: recommended revised circuit for unity-gain, non-inverting applications in new and revised designs. CWYLSO† . . . The 2S80 monolithic Resolver-to-Digital Converter is now available for /883 applications in the D package, as well as LCCs . . . In the Application Note, "Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters" (April 1988), there is an error in the diagram of a two-speed (32:1) system using the 2S80 and 2S81. CWYLSO† . . . AD9501 Digitally Programmable Delay Generator has the following additional specifications under DIGITAL INPUTS (full temperature range, test level VI): Latch Input "1" voltage (min), 2.0 V (J) and 2.3 V (S, mil subgroups 7,8); and Latch Input "0" voltage (max), 0.8 V, all versions. Also, the DIGITAL OUTPUT logic "0" voltage spec for the S version is changed to 0.45 max . . . Most versions of AD202, AD204, AD210, 1B21, 1B22, 1B41, 1B51, AD1170 now have 0.018"-square pins and a plastic pin header for easier handling and the ability to withstand higher shock and vibration. CWYLSO† . . . Lower prices on high-speed op amps in the AD840 series and the AD5539, as well as the ADOP07, ADOP27, ADOP37, AD518, and AD741. In fact, if you haven't checked our prices on these and other products recently, do so; you may be pleasantly surprised. CWYLSO†

**MILITARY ROLL CALL:** . . . The following Standard Military Drawing (SMD) products listed with "C" suffixes in the 1990 Military Products Data Book (see facing page) should now have "A" suffixes: 5962-: 85127013, 85127023, 8686101X, 8686102X, 8686103X, 87540012, 87789012, 87789022, 88659013, 89728012, 89728022, since the lead-finish specification has changed from gold to hot solder dip . . . New since publication of the Military Products DataBook: SMD 5962-898250 for the AD587 High-Precision 10-Volt Reference . . . SMD 5962-86716 (for the ADG201HS quad SPST switch) omits some important information included on the data sheet critical to its survival with ±17-volt inputs. CWYLSO† . . . For information on recently released reliability reports, CWYLSO†.

**SHOWS** . . . Come see us at: . . . SIGGRAPH, in Dallas TX, 6-10 August, 1990 . . . AES, in Los Angeles, 22-25 September, 1990 . . . Convergence, in Dearborn MI, 15-17 October, 1990 . . . RF Expo East, in Orlando FL, 13-15 November, 1990.

**PATENTS RECEIVED:** . . . 4,800,524 to John P. Roegen for Modulo Address Generator . . . 4,855,684 to Moshe Gerstenhaber and Robert J. Libert for Bias Current Compensation for Bipolar Input Stages . . . 4,859,944 to Spencer Webb for Single-Winding Magnetometer with Oscillator Duty Cycle Measurement . . . 4,891,533 to Peter R. Holloway for MOS-Cascoded Bipolar Current Sources in Non-Epitaxial Structure . . . 4,891,645 to Stephen R. Lewis and Scott A. Lefton for Digital-to-Analog Converter with on-Board Unity-Gain Inverting Amplifier . . . 4,899,152 to Jeff Barrow and Adrian P. Brokaw for Method and Apparatus for Temperature Compensating a Digital-to-Analog Converter . . . 4,902,959 to Adrian P. Brokaw for Band-Gap Voltage Reference with Independently Trimmable TC and Output.

\*Use the reply card for technical data.

†CWYLSO = Check with your local sales office

## IN THE LAST ISSUE

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Editor's Notes, Authors

*Monolithic 75-MSPS, 10-bit Flash Converter* (AD9020/9060)

*Wideband current-feedback Op Amps with low distortion* (AD9617/18)

*Macromodel of the AD9617*

*Considerations in choosing digital signal-processor architecture*

*14-bit dual-channel Synchronizer/Resolver-to-Digital Converter* (AD2S44)

*12-bit, 100-kbps complete Sampling-A/D-Converter ICs* (AD7875/7876)

*Low-drift, high-linearity Isolation Amplifier* (AD208)

*Computer Interface Panel handles eight analog outputs* (STB-AOT)

*Real-World Interface Cards for Micro Channel systems* (RTI-220/222)

New-Product Briefs:

Op Amp combines low offset voltage, bias current, & drift (AD705)

Register File has 5 16-bit ports, supports 40-MFLOPS μcoded DSP

Software support tools for ADSP-2101 (ADDS-2101-SW)

14-16-bit Digital-to-Resolver Converters: ±1' accuracy (AD2S65/66)

50-MB/s Disk-Drive Data Qualifier: 3 qualification levels (AD891A)

24-channel Digital Input/Output for 6B Series

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Potpourri (Last Issue, Errata, Timely Topics, Product Notes, MIL, Patents)

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